3.8V-32V Vin, 500KHz, 2A Synchronous Step-down DCDC Converter with EMI Reduction

- EMI Reduction with Switching Node Ringing-free
- 3.8V-32V

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NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision 1.0: Release to market

Revision 1.1: Add low side FET leakage in EC table

Revision 1.2: Format adjustment

Revision 1.3: Update Device Order Information

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GND	7	Power ground. Must be soldered directly to ground plane.
SW	8	Switching node of the buck converter.

Over operating free-air temperature range unless otherwise noted

PARAMETER **DEFINITION**

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V_{IN}=12V, T_J=-40°C~125°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply and Output						
V_{IN}						

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Figure 1. Efficiency, Vout=5V

Figure 2. VIN UVLO vs Temperature

Figure 3. Shut down

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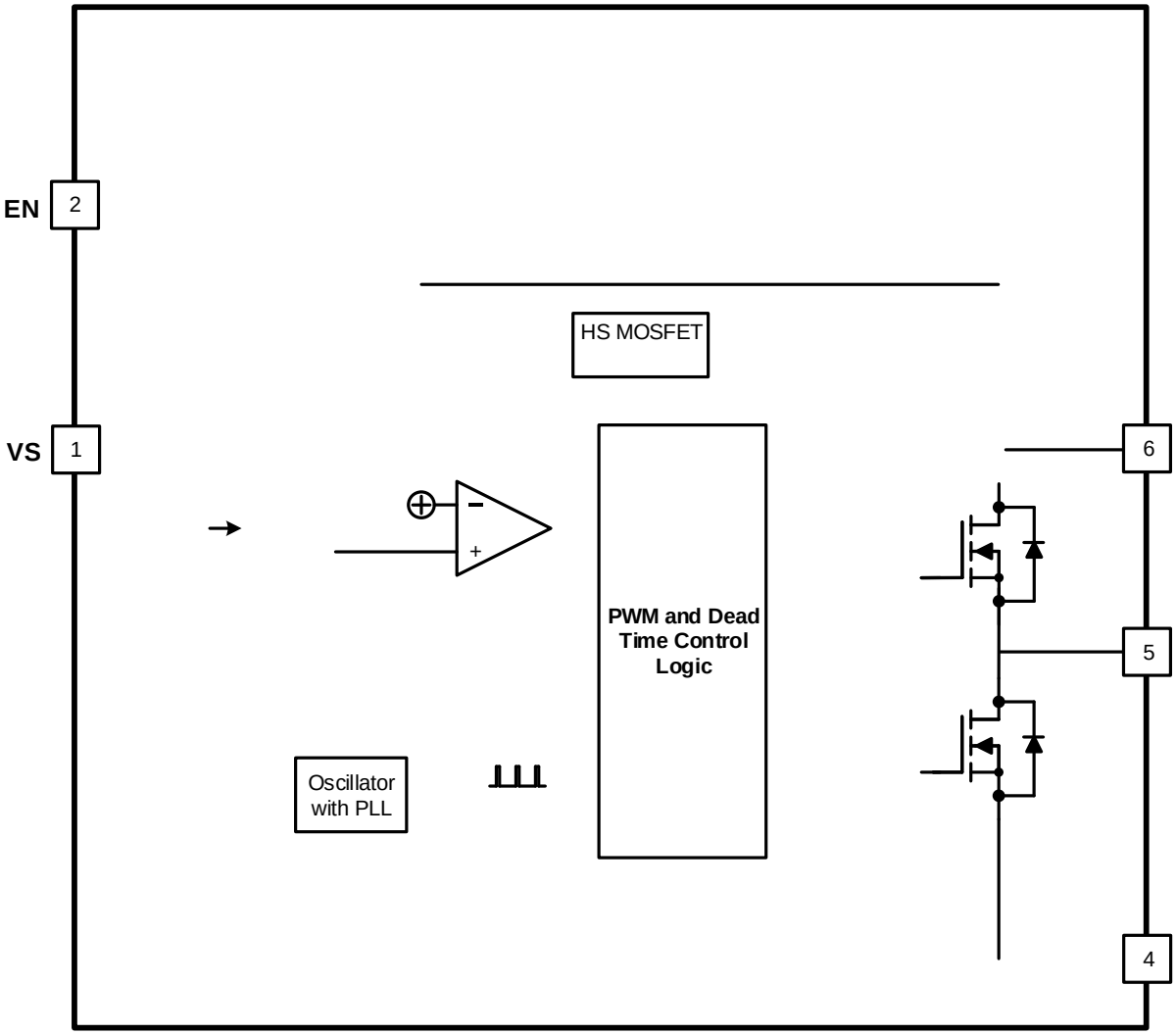

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Overview

The SCT9325

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band and therefore reduces conducted and radiated interference peak amplitude at a particular frequency. The SCT9325 feature 500KHz switching frequency with spreading frequency of +/-6% and modulation rate 1/512 of switching frequency. The FSS technique effectively decreases the EMI noise by spreading the switching frequency from fixed 500KHz. As a result, the harmonic wave amplitude is reduced and the harmonic wave band is wider.

In buck converter, the switching node ringing amplitude and cycles are critical especially related to the high frequency radiation EMI noise. The SCT9325 implement the multi-level gate driver speed technique to achieve the switching node ringing-free without scarifying the switching node rise/fall slew rate and

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Input Capacitor Selection

For good input voltage filtering, choose low-ESR ceramic capacitors. A ceramic capacitor 10 for the decoupling capacitor and a 0.1 to be placed as close as possible to the VIN pin of the SCT9325.

Use Equation (3) to calculate the input voltage ripple:

$$\Delta V_{IN} = \frac{I_{OUT}}{C_{IN} \times f_{SW}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (3)$$

Where:

- C_{IN} is the input capacitor value
- f_{sw} is the converter switching frequency
- I_{OUT} is the maximum load current

Due to the inductor current ripple, the input voltage changes if there is parasitic inductance and resistance between the power supply and the VIN pin. It is recommended to have enough input capacitance to make the input voltage ripple less than 100mV. Generally, a 35V/10uF input ceramic capacitor is recommended for most of applications. Choose the right capacitor value carefully with considering high-capacitance ceramic capacitors DC bias effect, which has a strong influence on the final effective capacitance.

Inductor Selection

The performance of avior, loop stability, and buck converter efficiency. The inductor value, DC resistance (DCR), and saturation current influences both efficiency and the magnitude of the output voltage ripple. Larger inductance value reduces inductor current ripple and therefore leads to lower output voltage ripple. For a fixed DCR, a larger value inductor yields higher efficiency via reduced RMS and core losses. However, a larger inductor within a given inductor family will generally have a greater series resistance, thereby counteracting this efficiency advantage.

Inductor values can have ±20% or even ±30% tolerance with no current bias. When the inductor current approaches saturation level, its inductance can decrease 20% to 35% from the value at 0-A current depending on how the inductor vendor defines saturation. When selecting an inductor, choose its rated current especially the saturation current larger than its peak current during the operation.

To calculate the current in the worst case, use the maximum input voltage, minimum output voltage, maxim load current and minimum switching frequency of the application, while considering the inductance with -30% tolerance and low-power conversion efficiency.

For a buck converter, calculate the inductor minimum value as shown in equation (4).

$$L_{MIN} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times I_{OUT} \times K_{IND}} \quad (4)$$

Where:

- K_{IND} is the coefficient of inductor ripple current relative to the maximum output current.

Therefore, LPEAK,

$$I_{LPEAK} = I_{OUT} \times K_{IND} + \frac{V_{OUT}}{2} \quad (5)$$

Set the current limit of the SCT9325 higher than the peak current I_{LPEAK} and select the inductor with the saturation current higher than the current limit. The the core loss significantly affect the efficiency of power conversion

ing current of inductor, I is calculated as in equation (5),

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- G_{MP} is the gain from internal COMP to inductor current, which is 5A/V.
- f_C is the cross over frequency.

Additional capacitance de-rating for aging, temperature and DC bias should be factored in which increases this

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Application Waveforms

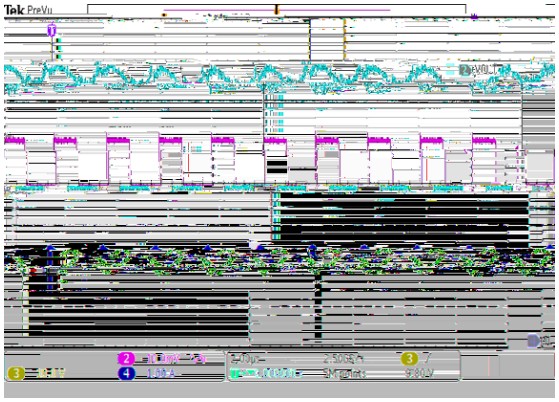

Figure 11. SW node waveform and Output Ripple, Iout=2A

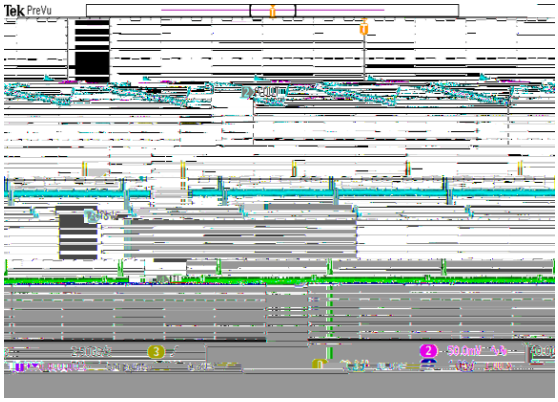

Figure 12. SW node Waveform and Output Ripple, Iout=10mA

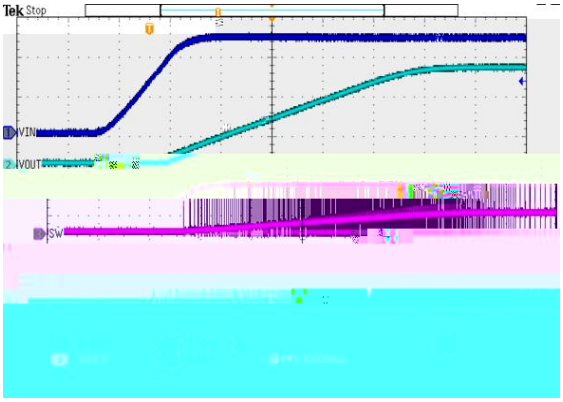

Figure 13. Power Up, Iout=10mA

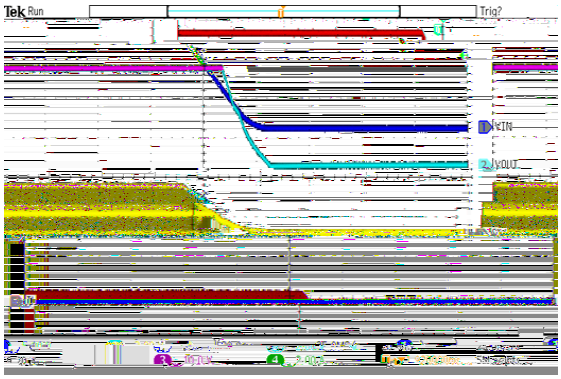

Figure 14. Power Down, Iout=10mA

Figure 15. Load Transient
(Vout=5V, Iout=0.2A to 1.8A, SR=250mA/us)

Figure 16. Load Transient
(Vout=5V, Iout=0.5A to 1.5A, SR=250mA/us)

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Layout Guideline

The regulator could suffer from instability and noise problems without carefully layout of PCB. Radiation of high-frequency noise induces EMI, so proper layout of the high-frequency switching path is essential. Minimize the length and area of all traces connected to the SW pin, and always use a ground plane under the switching regulator to minimize coupling. The input capacitor needs to be very close to the VIN pin and GND pin to reduce the input supply ripple. Place the capacitor as close to VIN pin as possible to reduce high frequency ringing voltage on SW

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