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NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision 1.0: Released to Production
Revision 1.3: Update package information, ABS max, add EC table max limit
Revision 1.4: Format adjustment
Revision 1.5: Correct package information in Page 16
Revision 1.6: Correct operating junction temperature
Revision 1.7: Update DEVICE ORDER INFORMATION

ORDERABLE DEVICE	PACKAGING TYPE	STANDARD PACK QTY	PACKAGE MARKING	PINS	PACKAGE DESCRIPTION

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VDD	6	Power Supply, must be locally bypassed by the ceramic cap.

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V_{DD}=

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D

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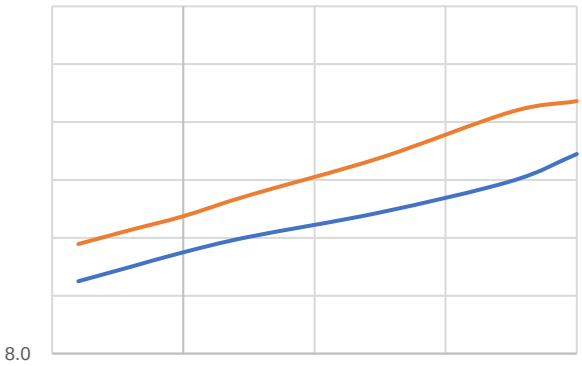

Figure 7. Input to Output Propagation Delay vs Temperature

Figure 8. ROH vs Temperature

Figure 9. ROL vs Temperature

Figure 10. Operation Supply Current vs Frequency, C_{OUT}=1nF

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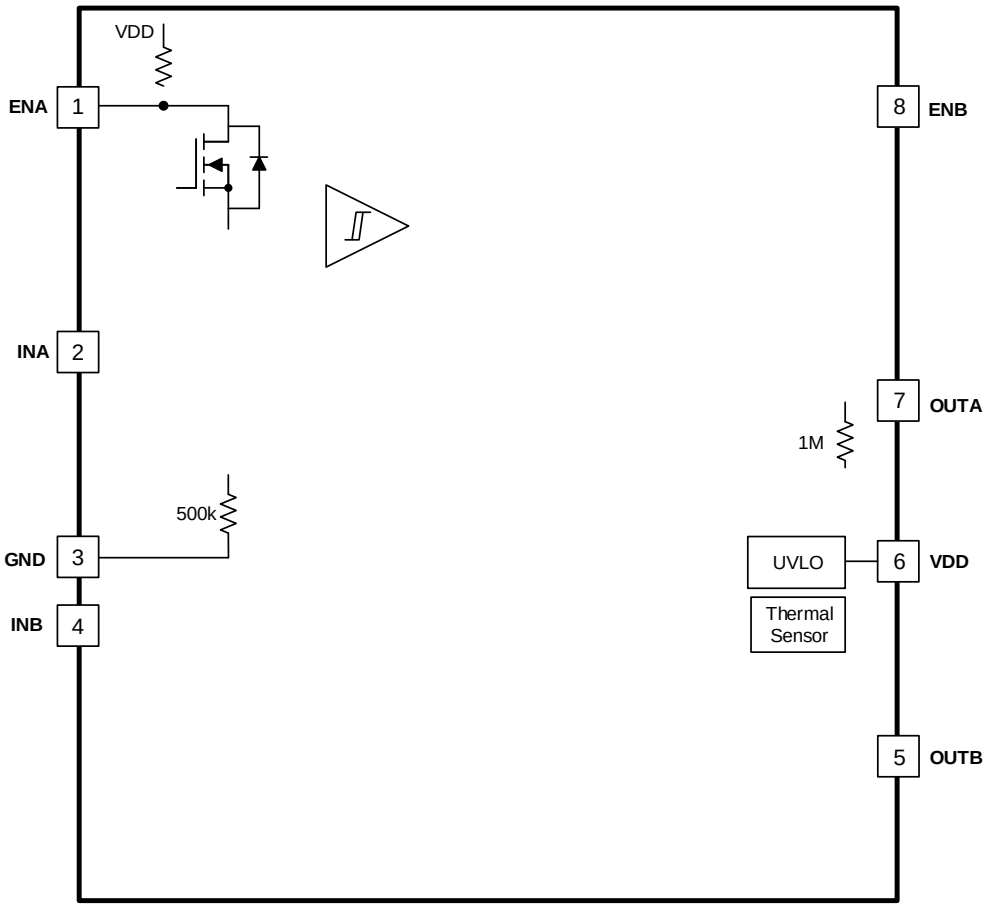

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Overview

The SCT52240 is a dual-channel non-invertible high-speed low side driver with supporting up to 24V wide supply for both power MOSFET and IGBT. Each channel can source and sink 4A peak current along with the minimum propagation delay 13ns from input to output. The 1ns delay matching and the stackable output characteristics support higher driving capability demanding in high power converter application. The ability to handle -5V DC input increases the noise immunity of driver input stage, the 24V rail-to-rail output

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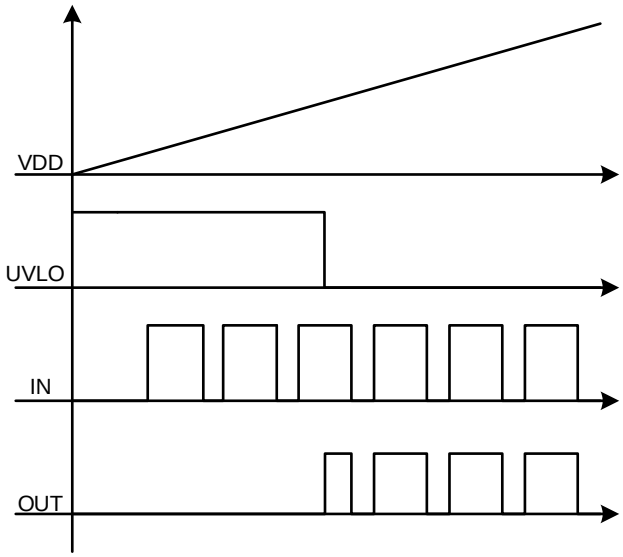

Figure 11. SCT52240 Output Vs VDD

Enable Function

SCT52240 provides independent enable pins ENA and ENB for external control of each channel operation. The enable pins are based on a TTL compatible input-threshold logic that is independent of the supply volta0 Gge and is effectively controlled with logic signals from 3.3-V and 5-V microcontrollers0 W. When applying a voltage higher than the high threshold (typical 2.1V) the pin, the SCT52240 enables all functions and starts gate driver operation. Driver operation is disabled when ENx voltage fa0 Gbs below its lower threshold (typical 1V). The ENx pins are internally pulled up to VDD with 4 00k pullup resistors. Hence, the ENx pins can be left floating or Not Connected (N/C) for standard operation, where the enable feature is not required.

Input Stage

The input ofSCT52240 is compatible on TTL input-threshold logic that is independent of the VDD supply voltage. With typically high threshold = 2.1 V and typically low threshold = 1 V, the logic level thresholds are tyen-USEN

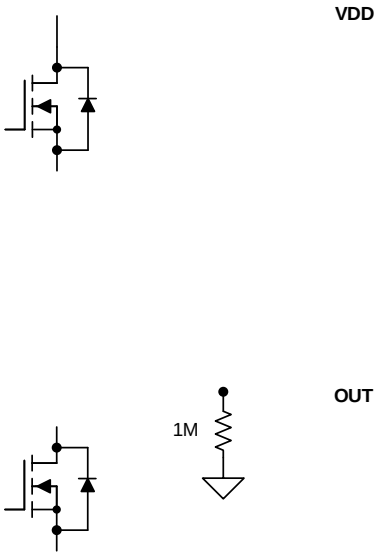

Figure 12. SCT52240 Output Stage

Stackable Output

The SCT52240 features 1ns (typical) delay matching between dual channels, which enables dual channel outputs be stackable when the driven power device required higher driving capability. For example, in a Boost Power Factor Correction converter, there are 2 power MOSFET in parallel to support higher power output capability. The two power MOSFET are preferred to be driven by a common gate control signal. By using f3,4(CT)-32(f3,24(4)4,(e)-34(t)-1heng)4

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Typical Application

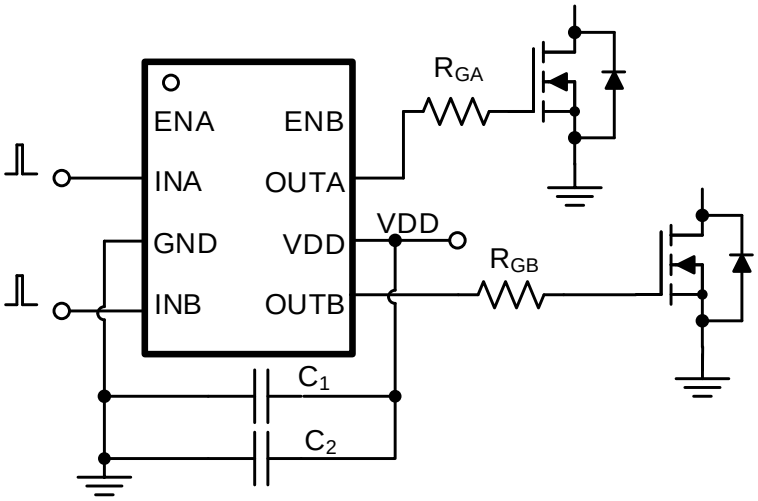

Figure 16. Dual Channel Driver Typical Application

Driver Power Dissipation

Generally, the power dissipated in the SCT52240 depends on the gate charge required of the power device (Qg), switching frequency, and use of external gate resistors. The SCT52240 features very low quiescent currents and internal logic to eliminate any

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(3)

Where

- R_{OH} is the equivalent pull up resistance of SCT52240
- R_{OL} is the pull down resistance of SCT52240
- R_G is the gate resistance between driver output and gate of power device.

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Application Waveforms

Figure 17. Driver Switching ON

Figure 18. Driver Switching OFF

Figure 19. Delay Matching Rise

Figure 20. Delay Matching Fall

Figure 21.

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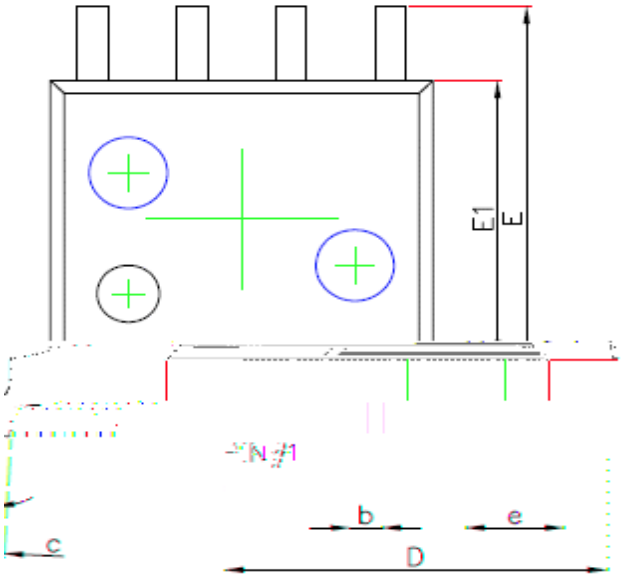
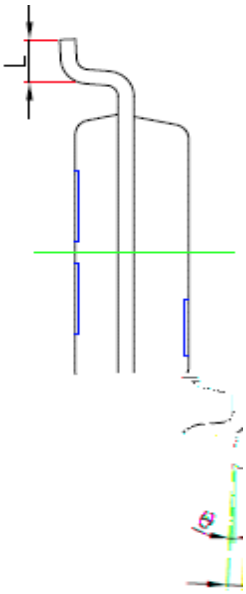
Layout Guideline

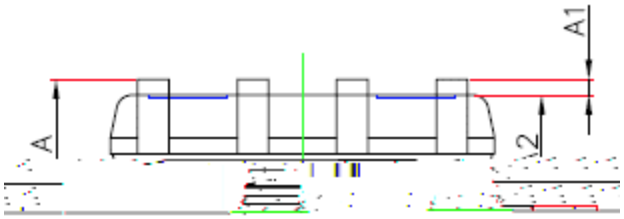
The SCT52241[illegible]



TOP VIEW



BOTTOM VIEW



SIDE VIEW

SYMBOL	Unit: Millimeter		
	MIN	TYP	MAX
A	1.45	---	1.75
A1	0.1	---	0.25
A2	1.35	---	1.55
b	0.33	---	0.51
c	0.17	---	0.25
D	4.7		5.1
E	5.8		6.2
E1	3.8		4.0
e	1.27BSC		
L	0.4		1.27
	0°		8°

NOTE:

1. Drawing proposed to be made a JEDEC package outline MO-220 variation.
2. Drawing not to scale.
3. All linear dimensions are in millimeters.
4. Thermal pad shall be soldered on the board.
5. Dimensions of exposed pad on bottom of package do not include mold flash.
6. Contact PCB board fabrication for minimum solder mask web tolerances between the pins.

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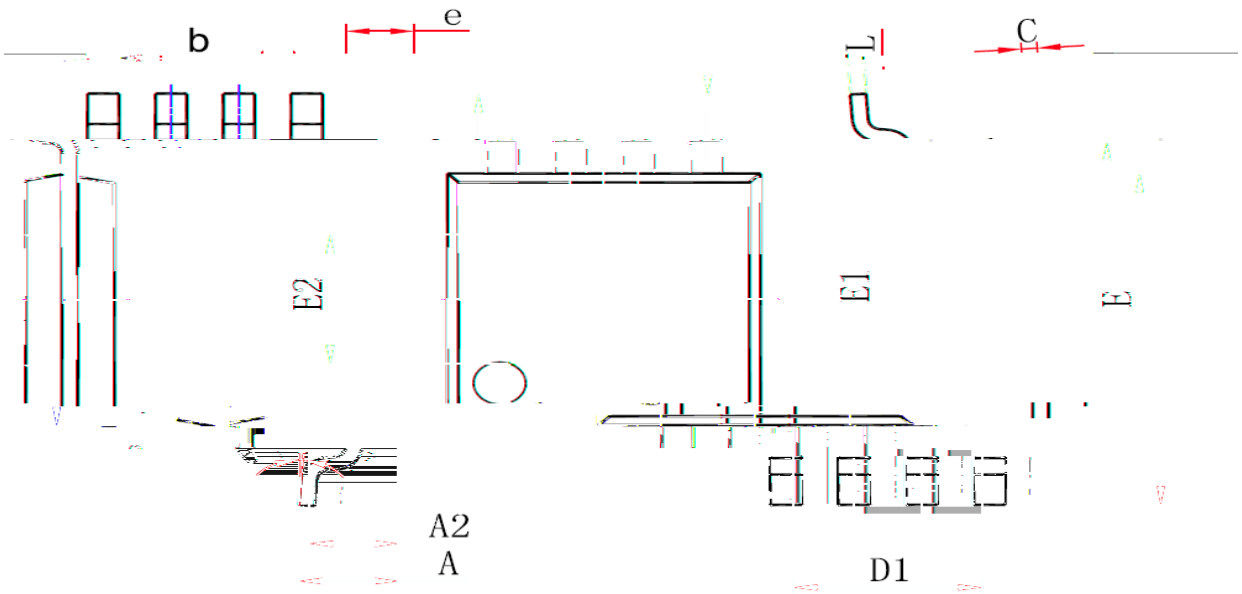
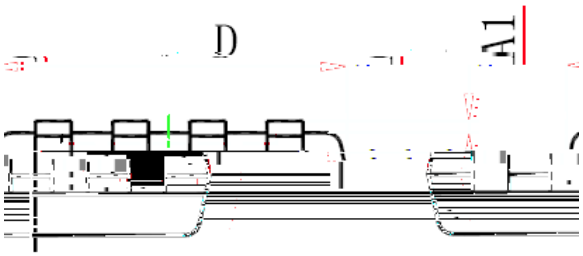


TOP VIEW

BOTTOM VIEW



SIDE VIEW

SYMBOL	Unit: Millimeter		
	MIN	TYP	MAX
A	0.82	---	1.1
A1	0.02	---	0.15
A2	0.75	---	0.95
b	0.25	---	0.38
c	0.09	---	0.23
D	2.9		3.1
D1	1.7		1.9
E	2.9		3.1
E1	4.75		5.05
E2	1.45		1.65
e	0.65BSC		
L	0.4		0.8
	0°		6°

NOTE:

7. Drawing proposed to be made a JEDEC package outline MO-220 variation.
8. Drawing not to scale.
9. All linear dimensions are in millimeters.
10. Thermal pad shall be soldered on the board.
11. Dimensions of exposed pad on bottom of package do not include mold flash.
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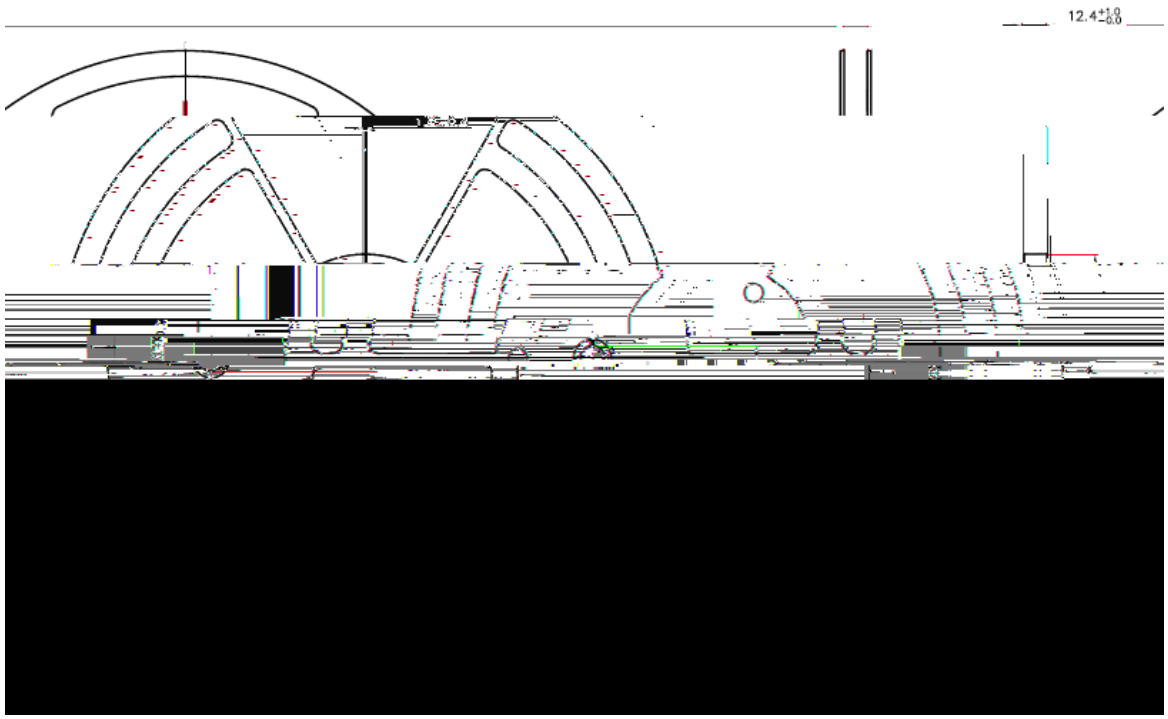

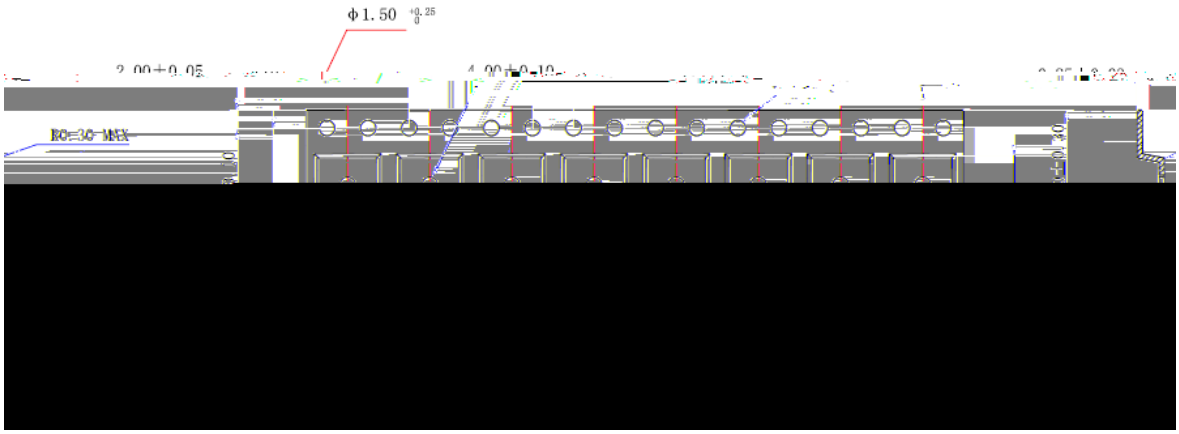

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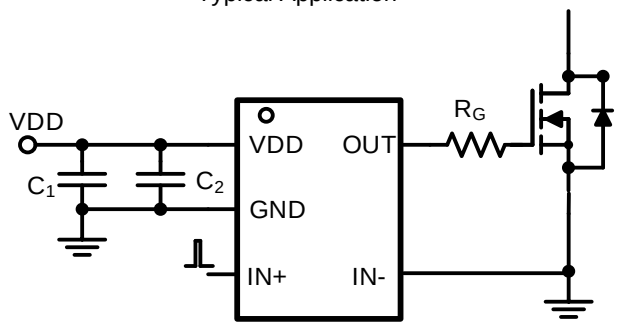
Single Channel, Non-Inverting MOSFET Gate Drive
Typical Application



Typical Application Waveform

PART NUMBERS **DESCRIPTION** **COMMENTW*nBTF1 9Tf1 0 0**