 © 2019

REVISION HISTORY

 © 2020 Silicon Content Technology Co., Ltd. All Rights Reserved

VIN	5	Power supply input. Must be locally bypassed.
SW	6	Switching node of the buck converter.

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range unless otherwise noted

V_{IN}	Input voltage range	4.5	40	V
T_J	Operating junction temperature	-40	125	°C

ESD RATINGS

V_{ESD}	Human Body Model (HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins(1)	-2	+2	kV
	Charged Device Model (CDM), per ANSI-JEDEC-JS-002-2014specification, all pins(1)	-0.5	+0.5	kV

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2)

 © 2020 Silicon Content Technology Co., Ltd. All Rights Reserved

 © 2020 Silicon Content Technology Co., Ltd. All Rights Reserved

 © 2020 Silicon Content Technology Co., Ltd. All Rights Reserved

TYPICAL CHARACTERISTICS

Figure 7. LS Current Limit VS Temperature

Figure 8. Quiescent Current vs Temperature VIN=12V

Figure 9. Shutdown Current vs Temperature, Vin=24V

Figure 10. EN Threshold vs Temperature

Figure 11. VIN UVLO VS Temperature

Figure 12. OVP VS Temperature

 © 2020 Silicon Content Technology Co., Ltd. All Rights Reserved

FUNCTIONAL BLOCK DIAGRAM

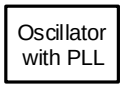


Figure 13. Functional Block Diagram

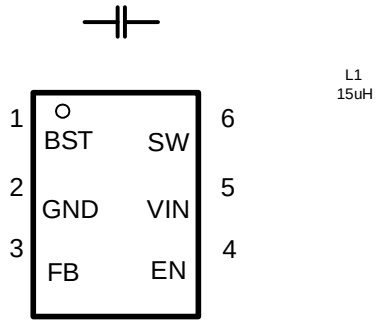
 © 2020 Silicon Content Technology Co., Ltd. All Rights Reserved

 © 2020 Silicon Content Technology Co., Ltd. All Rights Reserved

 © 2020 Silicon Content Technology Co., Ltd. All Rights Reserved

For more information

APPLICATION INFORMATION



[redacted]

 © 2020 Silicon Content Technology Co., Ltd. All Rights Reserved

The output voltage is set by an external resistor divider R1 and R2 in typical application schematic. Recommended R2 resistance is 20KΩ

 © 2020 Silicon Content Technology Co., Ltd. All Rights Reserved

 © 2020 Silicon Content Technology Co., Ltd. All Rights Reserved

Unless otherwise noted the following conditions apply: Vin=24V, VOUT=12V, F_{SW}=2000kHz.

Figure 19. Power up

Figure 20. Power down

Figure 21

 © 2020 Silicon Content Technology Co., Ltd. All Rights Reserved

The regulator could suffer from instability and noise problems without carefully layout of PCB. Radiation of high-frequency noise induces EMI, so proper layout of the high-frequency switching path is essential.

1. Minimize the length and area of all traces connected to the SW pin, and always use a ground plane under the switching regulator to minimize coupling.
2. The input capacitor needs to be very close to the VIN pin and GND pin to reduce the input supply ripple. Place a low ESR ceramic capacitor as close to VIN pin and the ground as possible to reduce parasitic effect.
3. Output inductor should be placed close to the SW pin. The area of the PCB conductor minimized to prevent excessive capacitive coupling.
4. The layout needs be done with well consideration of the thermal. A large top layer ground plate using multiple thermal vias is used to improve the thermal dissipation. The bottom layer is a large ground plane connected to the top layer ground by vias.

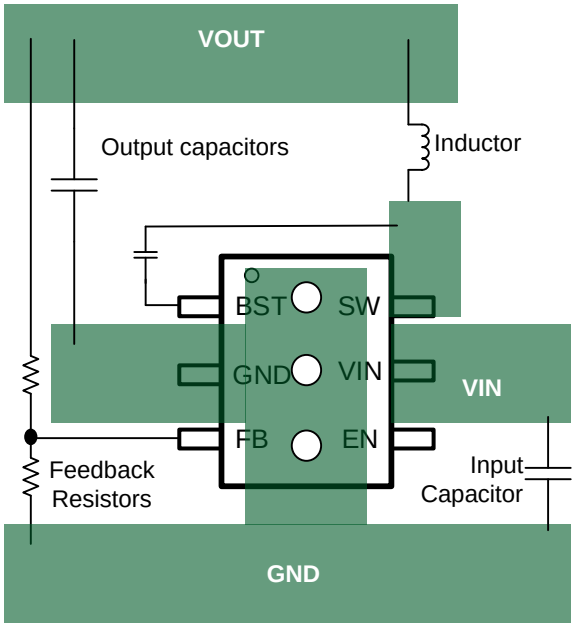
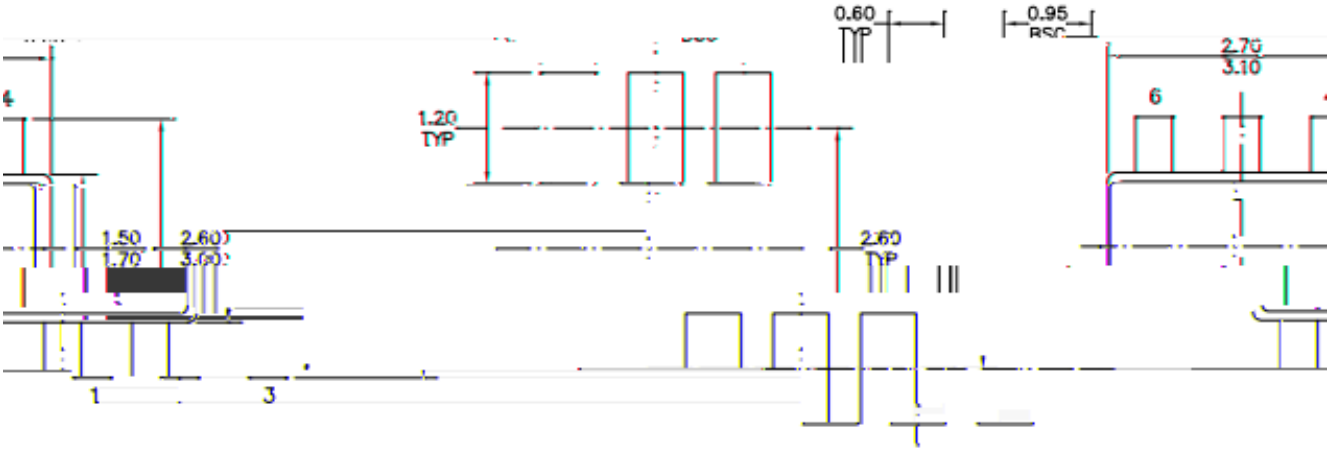


Figure 25. PCB Layout Example

 © 2020 Silicon Content Technology Co., Ltd. All Rights Reserved

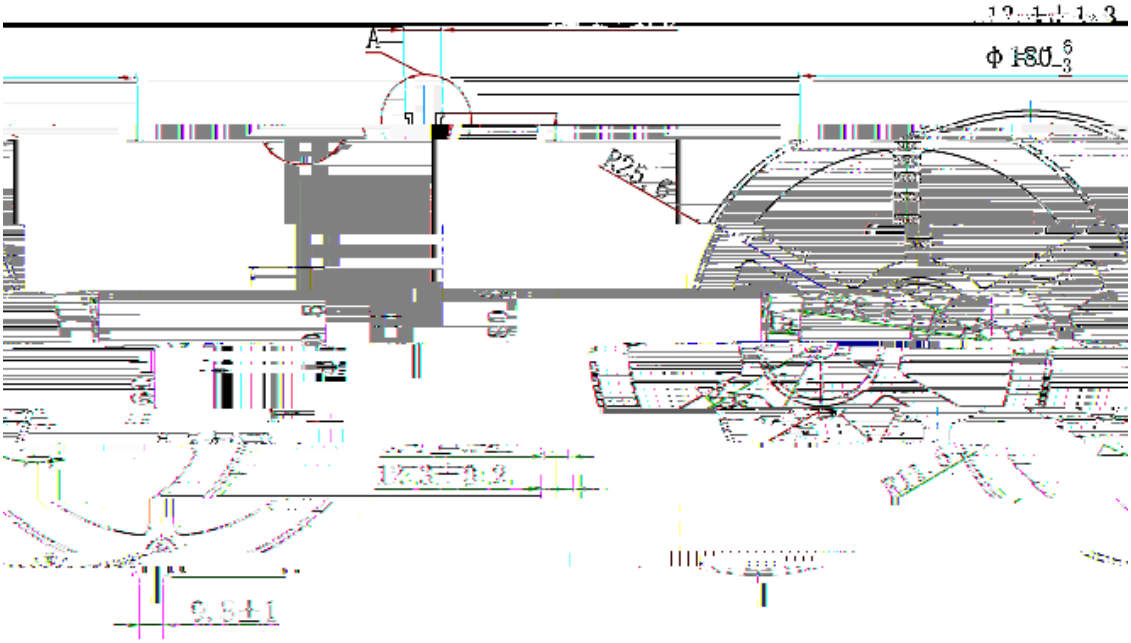
PACKAGE INFORMATION

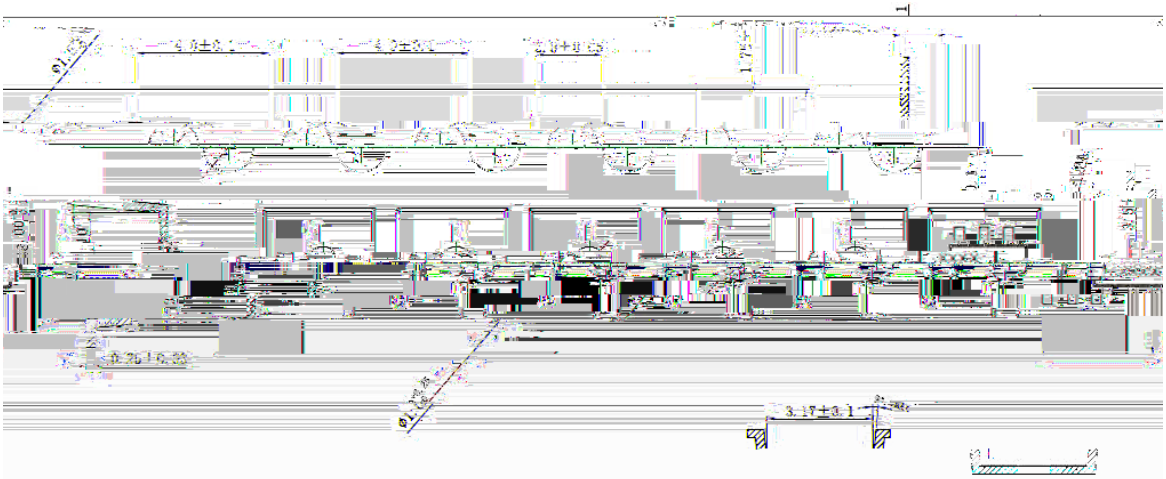


TOP VIEW **RECOMMENDED LAND PATTERN**

 © 2020 Silicon Content Technology Co., Ltd. All Rights Reserved

TAPE AND REEL INFORMATION





 © 2020 Silicon Content Technology Co., Ltd. All Rights Reserved