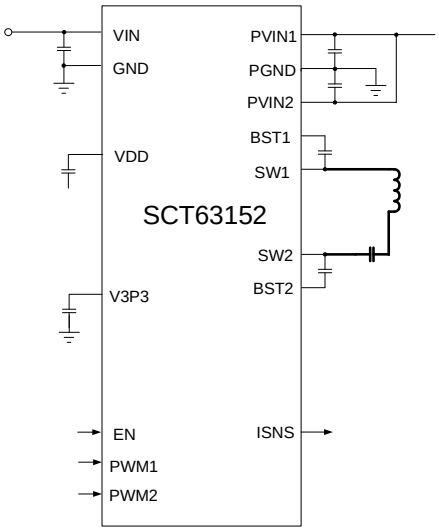

Low IQ mode quiescent current vs. Vin

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.
Revision 1.0: Released to Market.

ORDERABLE DEVICE	PACKAGING TYPE	STANDARD PACK QTY	PACKAGE quieE

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NAME	NO.	PIN FUNCTION
PVIN1	1	Input supply voltage of half-bridge FETs Q1 and Q2. Connected to the drain of high side FET Q1. A local bypass capacitor from PVIN1 pin to PGND pin should be added. Path from PVIN1 pin to high frequency bypass capacitor and PGND must be as short as possible.
PGND	3	PGND is the common power ground of the full bridge, connected to the source terminal of low side FETs Q2 and Q4 internally.
PVIN2	5	Input supply voltage of half-bridge FETs Q3 and Q4. Connected to the drain of high side FET Q3. A local bypass capacitor from PVIN2 pin to PGND pin should be added. Path from PVIN2 pin to high frequency bypass capacitor and PGND must be as short as possible.
VIN	6	Input supply voltage of the 5V LDO. Add a local bypass capacitor from VIN pin to GND pin. Path from VIN pin to high frequency bypass capacitor and GND must be as short as possible.
GND	7	
VDD	8	Output voltage of the 5V LDO. Connect 2.2uF capacitor from this pin to GND pin. VDD is the input power supply for gate driver of power stage and the 3.3V LDO.
V3P3		

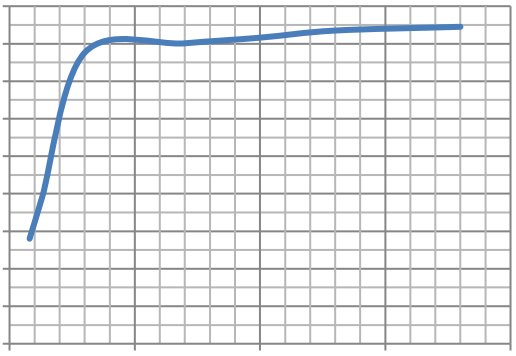

Figure 2. Low IQ mode current vs Vin

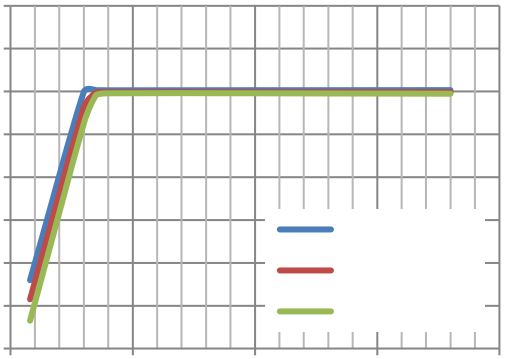

Figure 3. 5V LDO Vout vs Vin

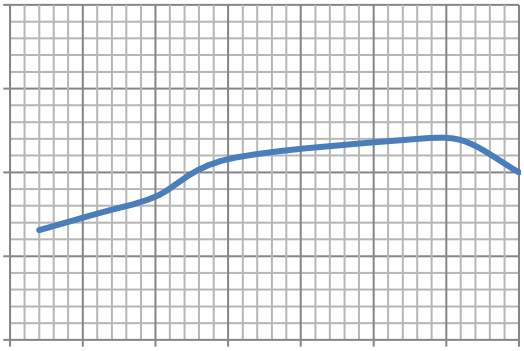

Figure 4. 5V LDO Vout vs temperature @Vin=12V

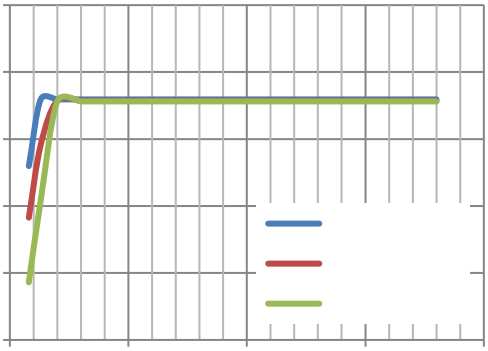

Figure 5. 3.3V LDO Vout vs Vin

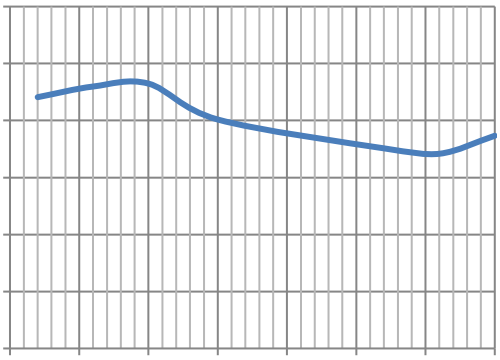

Figure 6. 3.3V LDO Vout vs temperature @Vin=12V

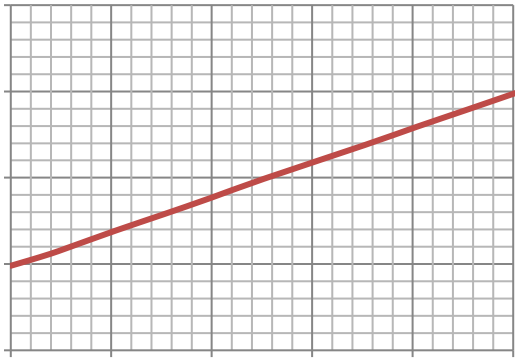

Figure 7. Current Sense Output Voltage vs Iin

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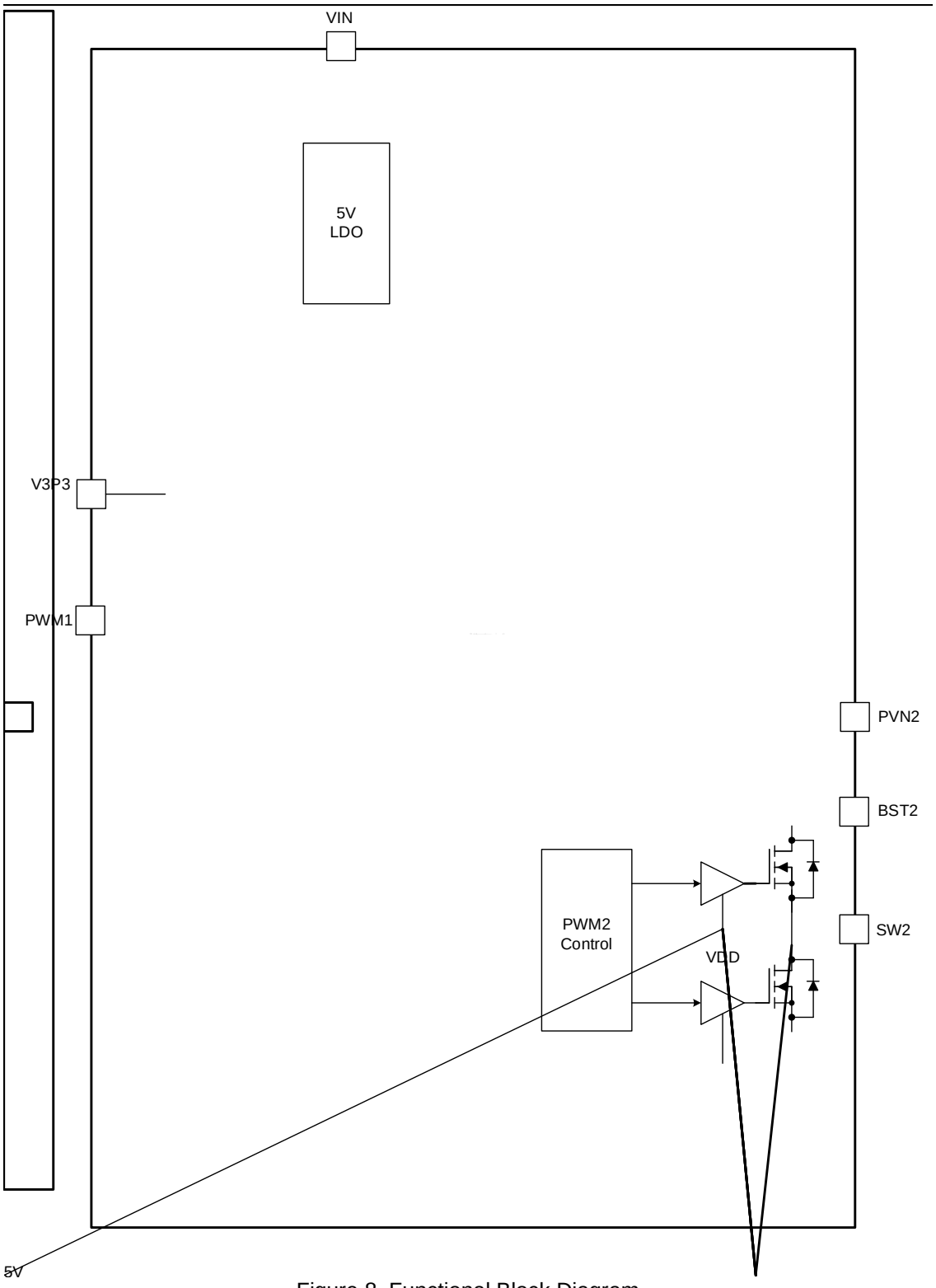

Figure 8. Functional Block Diagram

Overview

The SCT63152 is a highly integrated power management unit optimized for wireless power transmitter applications. This device integrates the power functions required to a wireless power transmitter including 5V

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PWM1 input controls the half bridge comprised of high side MOSFET Q1 and low side MOSFET Q2, and PWM2 input controls the half bridge comprised of high side MOSFET Q3 and low side MOSFET Q4 as shown in block diagram. The PWM1 and PWM2 independently control the SW1 and SW2 duty cycle and frequency. Logic HIGH will turn off low side FET and turn on high side FET, and logic LOW will turn off high side FET and turn on low side FET.

An external 100nF ceramic bootstrap capacitor between BST1 and SW1 pin powers floating high-side power MOSFET Q1's gate driver, and the other 100nF bootstrap capacitor between BST2 and SW2 pin powers for the Q3's. When low side FET is on which means SW is low, the bootstrap capacitor is charged through internal path by VDD power supply rail.

PWM cannot been kept as high level for more than 2ms since the voltage of bootstrap capacitor will be discharged by internal leakage current if high side FET keeps on.

Full Bridge Over Current Protection

The SCT63152 integrates cycle-by-cycle current limit and hiccup mode for over-current protection. The current of the high side FET Q1 and Q3 is sensed and compared to the current limit threshold during each switching cycle. If the current exceeds the threshold, 8A typical, the high side FET turns off immediately in present cycle to avoid current increasing even PWM signal is still kept in a high level. The over current counter is incremented. If one high side FET occurs over current in 5 consecutive cycles, then all 4 internal FETs are turned off regardless of the PWM inputs. The full bridge enters hiccup mode and will attempt to restart after a time-out period of 20ms typically.

Current Sense

The SCT63152

It is recommended to connect a decoupling ceramic capacitor of 1uF to 10uF to the V3V pin. Capacitor values outside of the range may cause instability of the internal linear regulator.

Low IQIQ

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Typical Application

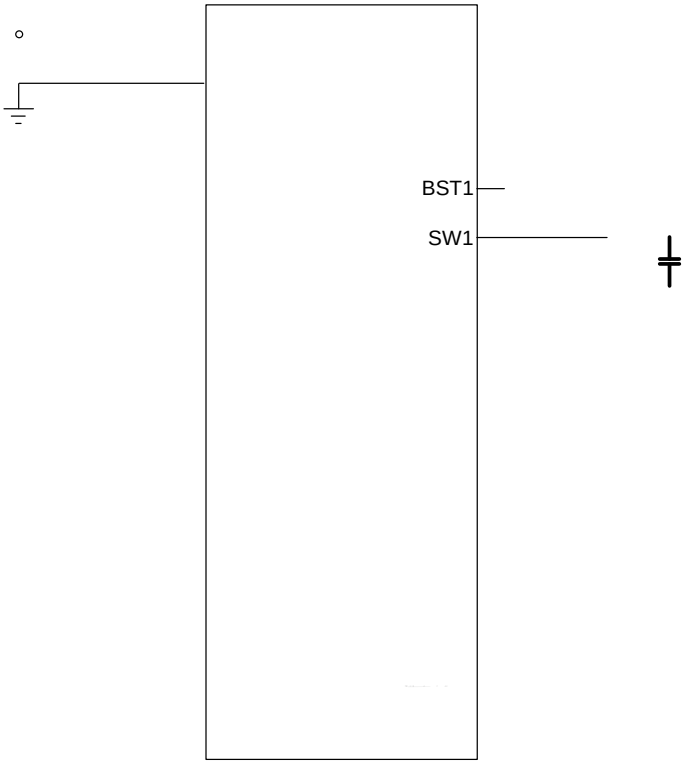

Figure 11. Same Input to VIN and PVIN

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Layout Guideline

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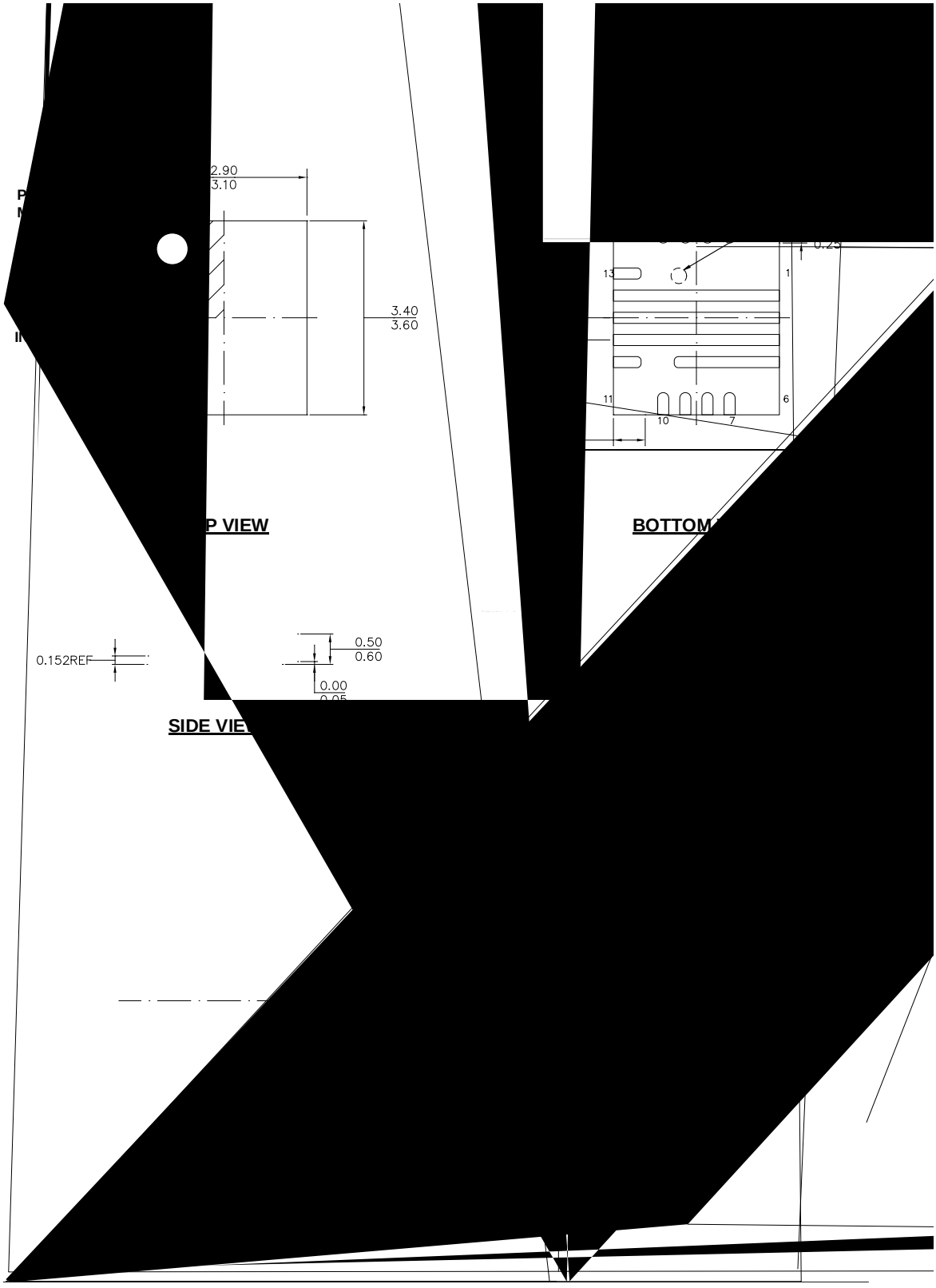
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