

G

NAME	NO.	DESCRIPTION
PGND	7	Power ground pin.
DR	8	N-channel MOSFET gate drive output. Connect directly to the gate of the N-channel MOSFET through a short, low inductance path.
VCC	9	Output of the internal VCC regulator and supply voltage input of the MOSFET driver. Connect a ceramic bypass capacitor from this pin to PGND.
VIN	10	Power supply input pin

V_{IN}=12V, T_J=-40℃~125℃, typical values are tested under 25℃.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT

Figure 1. I_{SD} vs. Input Voltage

Figure 2. I_Q vs. Input

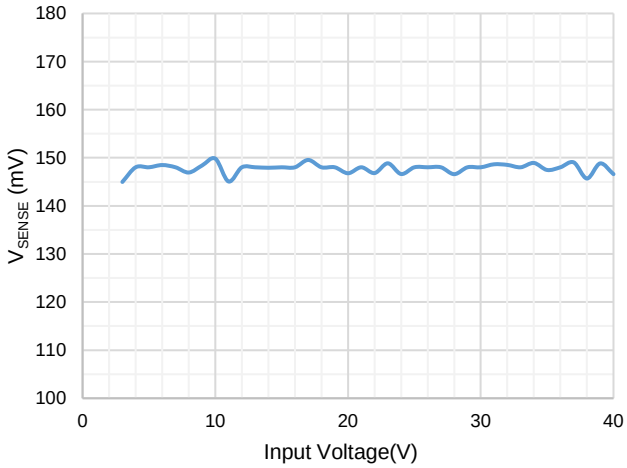

Figure 7. Current Sense Threshold vs. Input Voltage

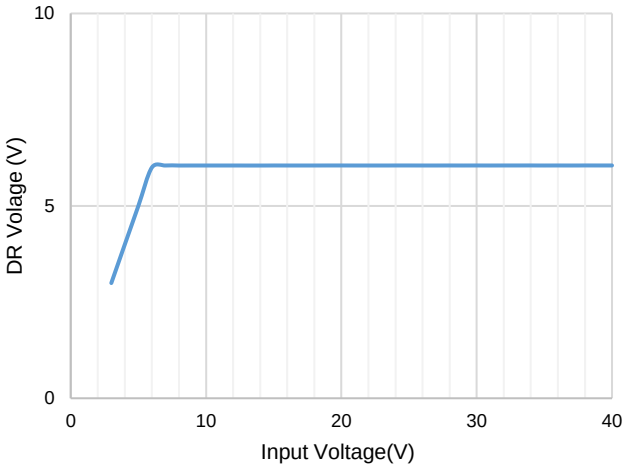

Figure 8. DR Volage vs. Input Voltage

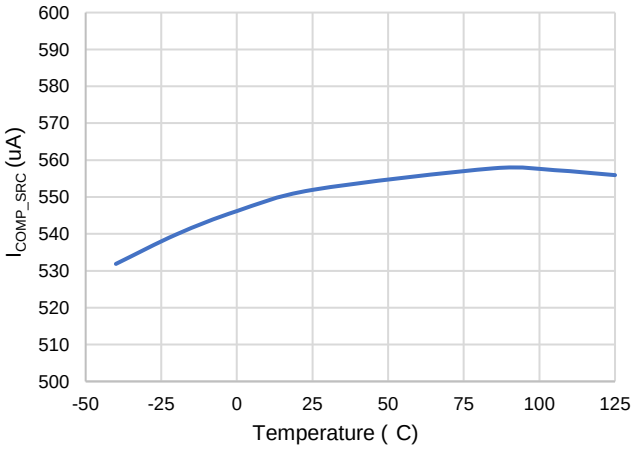

Figure 9. COMP Source Current vs. Temperature

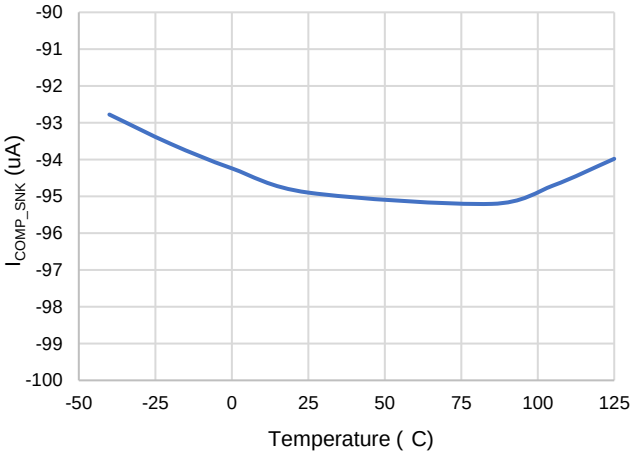

Figure 10. COMP Sink Current vs. Temperature

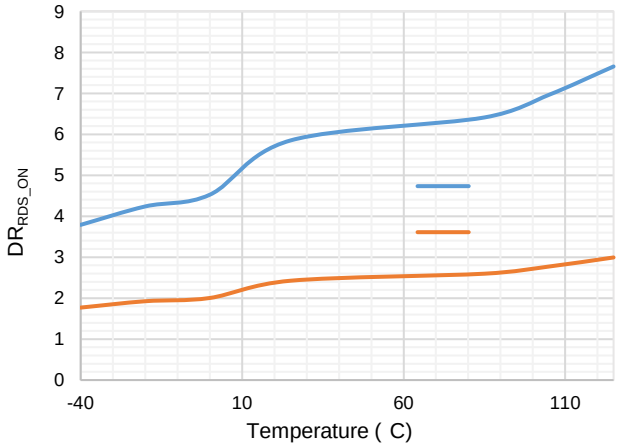

Figure 11. DR Resistance vs. Temperature

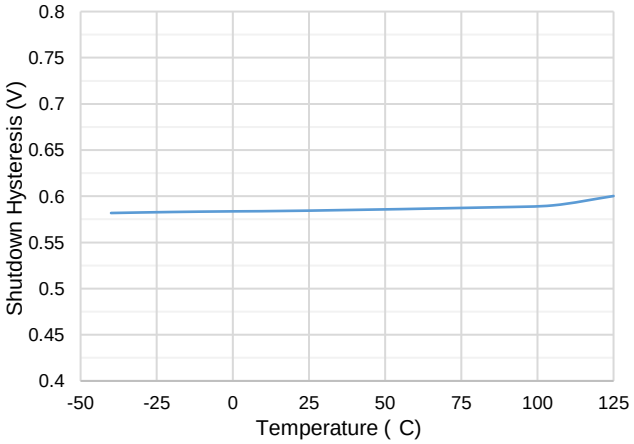

Figure 12. Shutdown Threshold Hysteresis vs. Temperature

G

Figure 13. Functional Block Diagram

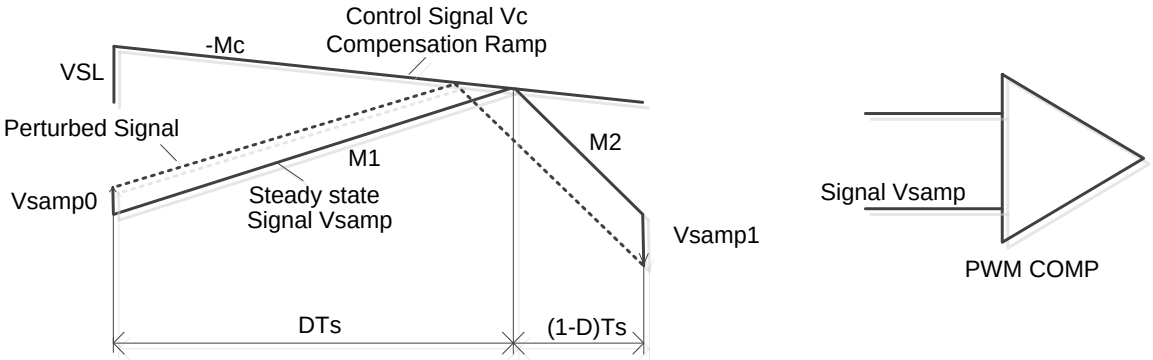

Figure 14. Sub-Harmonic Oscillation for D>0.5 and Compensation Ramp to Avoid Sub-Harmonic Oscillation

The current mode control scheme samples the inductor current, IL, and compares the sampled signal, V_{samp}, to a internally generated control signal, Vc. The current sense resistor, R_{SEN}, as shown in Figure 15 converts the sampled inductor current, IL, to the voltage signal, V_{samp}, that is proportional to IL such that

= (1)

The compensation ramp has been added internally in the SCT81624Q. The slope of this compensation ramp has been selected to satisfy most applications, and its value depends on the switching frequency. This slope can be calculated using the formula:

$$= \quad (9)$$

V_{SL} is the amplitude of the internal compensation ramp and F_S

Output Voltage

The output voltage is set by an external resistor divider RFBT and RFBB in typical application schematic. A minimum current of typical 20uA flowing through feedback resistor divider gives good accuracy and noise covering. The value of RFBT can be calculated by Equation 12.

$$= \frac{-}{} \times \quad (12)$$

where:

V_{REF} is the feedback reference voltage, typical 1.275V

Frequency Adjust/Shutdown/ Synchronization

The switching ntching ntchingThe switching en-US.iq000.Tf.6o0 g0 GSQ18.36 reW* ncal 20.00000912 0 612 792 reW* nBT/F3 9

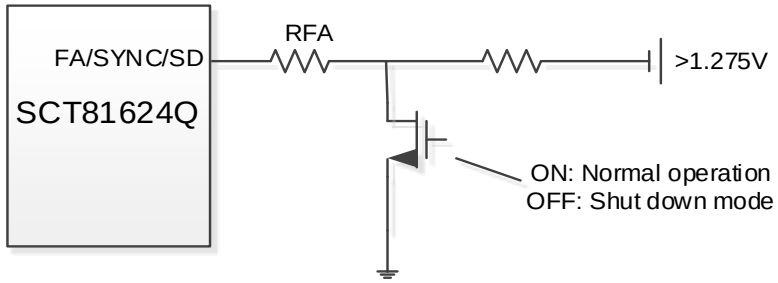

Figure18. Shutdown operation in Frequency Adjust Mode

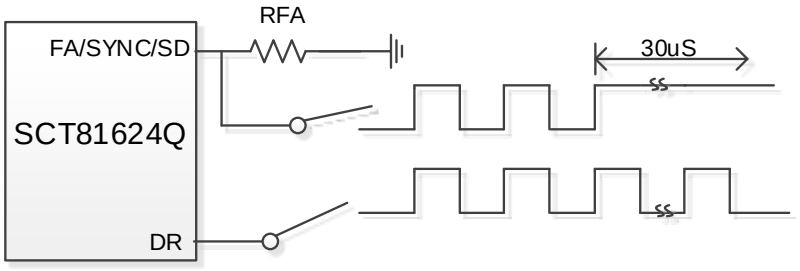

Figure19. Shutdown operation in Frequency Synchronization 3 Tm[p[o)]TJETQ EMC /Span <</MMCID 3/La

The input capacitor should be capable of handling the RMS current. Although the input capacitor is not as critical in a boost application, low values can cause impedance interactions. Therefore, a good quality capacitor should be chosen in the range of 10 µF to 40 µF. If a value lower than 10 µF is used, then problems with impedance interactions or switching noise can affect the SCT81624Q. To improve performance, especially with Vin below 8 volts, it is recommended to use a 2.2 Ohm resistor at the input to provide an RC filter. The resistor is placed in series with the VIN pin with only a bypass capacitor attached to the VIN pin directly. A 0.1-µF or 1-µF ceramic capacitor is necessary in this configuration. The bulk input capacitor and inductor will connect on the other side of the resistor at the input power supply.

Output Capacitor Selection

For small output voltage ripple, choose a low-ESR output capacitor like a ceramic capacitor. Typically, 3 4x 22 ceramic output capacitors work for most applications.
placed as close as possible to the switch node Higher capacitor values can be used to improve the load transient response. Due to derating under DC bias, the bias can significantly reduce capacitance. Ceramic

Where

$_G$ is the gate drive current.

The total power dissipation of MOSFET includes conduction loss as shown in the first term and switching loss as shown in the second term. The total power dissipation should be within package thermal ratings.

Output Diode Selection

Observation of the boost converter circuit shows that the average current through the diode is the average load

Application Waveforms
Vin=5V, Vout=12V, unless otherwise noted

Figure 22. Power up(Iload=2A)

Figure 23. Power down(Iload=2A)

Figure 24. Over current protection (Iload=5A)

Figure 25. Over current recovery (Iload=5A)

Figure 26. Steady-state

Typical Application(Sepic)

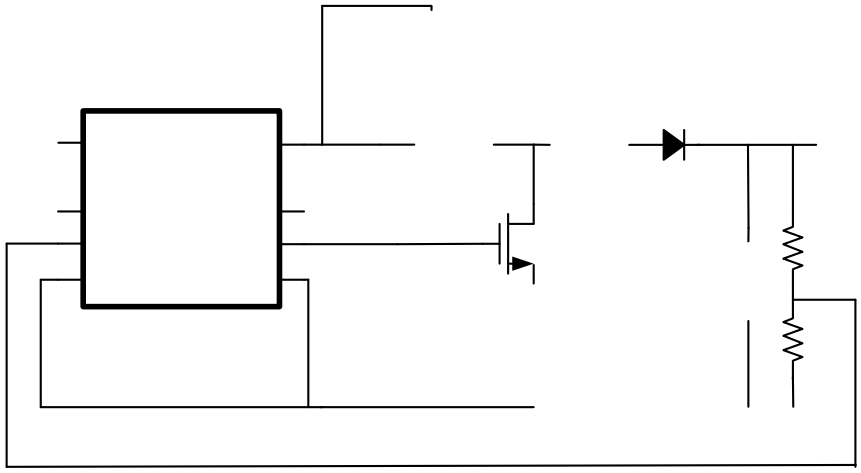

Figure 28. Application Schematic, 5V to 50V, 2A Sepic Regulator at 400kHz

Design Parameters

Design Parameters	Example Value
Input Voltage	24V Normal 5V to 50V
Output Voltage	12V
Maximum Output Current	2A
Switching Frequency	400

Inductor Selection (Sepic)

A good rule for determining the inductance to use is to allow the inductor peak-to-peak ripple current to be approximately 20% to 40% of the maximum input current at the minimum input voltage. The current ripple flowing in inductors L1 and L2 is given by:

$$\Delta = \times \times \frac{}{} \times \quad (27)$$

(28)

Normally we can select equal value for the inductors L1 and L2, derived as:

$$= = \frac{}{\Delta \times} \times \quad (29)$$

Where

$_{SW}$ is the switching frequency.

Note that the saturation current of inductors should be greater than peak current flowing in inductors, given by:

$$= + \frac{\Delta}{} = \times \frac{}{} \times + \frac{}{} \quad (30)$$

$$= + \frac{\Delta}{} = \times + \frac{}{} \quad (31)$$

If L1 and L2 are wound in same core as a coupled inductor, the inductance required will be half due to the mutual induction, calculated by:

$$= = - \frac{}{\times \Delta \times} \times \quad (32)$$

Power MOSFET Selection

The following parameters should be taken into consideration for MOSFET: the on-resistance R_{DS_ON}, the minimum gate threshold voltage V_{TH_MIN}, the total gate charge Q_g, the reverse transfer capacitance C_{RSS},

Output Diode Selection

The diode at the output side must withstand the reverse voltage when the MOSFET is turned-on. The peak reverse voltage is given by:

tage ripple on coupling c:

= + here 9763 00000934 2

The diode should also be capable to flow switch peak current I_{Q_PEAK}.

The power dissipation of the diode is equal to the forward voltage drop multiplies output current. Schottky diodes are recommended here to minimize the power loss.

Coupling Capacitor Selection

For ceramic capacitors with low-ESR, the peak to peak voltage ripple on coupling cn <</M

olMO

Application Waveforms

Vin=5V, Vout=12V, unless otherwise noted

Figure 30. Power up(Iload=2A)

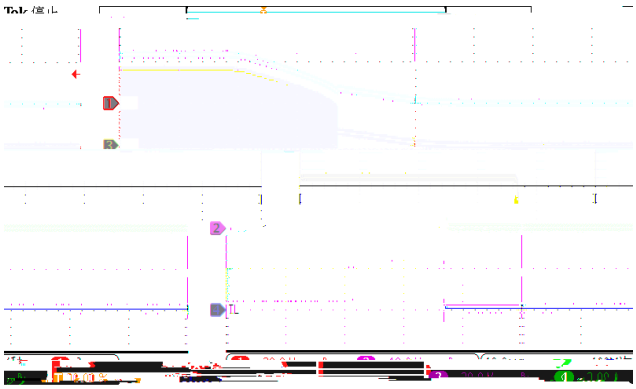

Figure 31. Power down(Iload=2A)

Figure 32. Shutdown entry

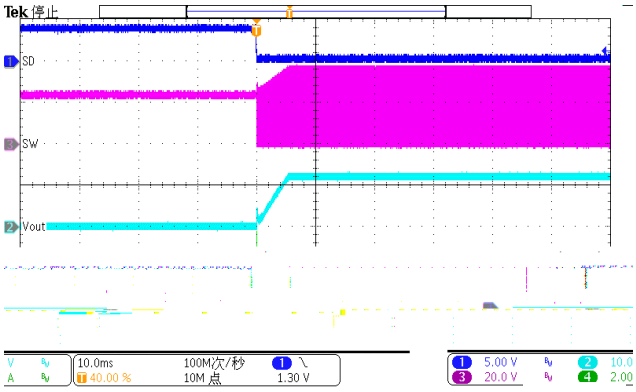

Figure 33. Shutdown remove

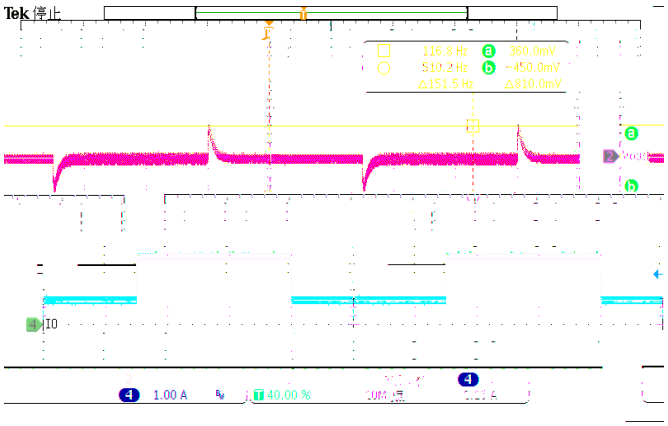

Figure 34. LoadTrans (Iload=0.5A-1.5A)

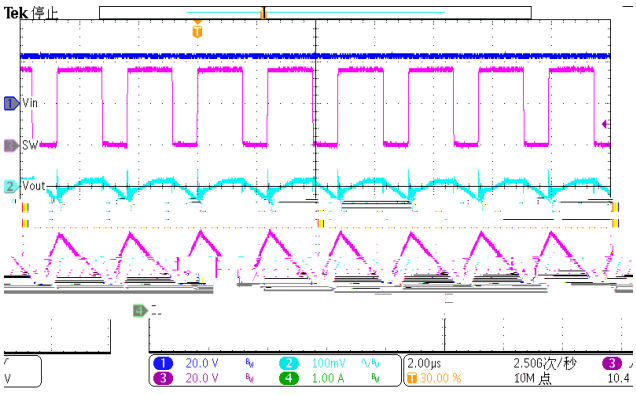

Figure 35. steady-state (Iload=2A)

Layout Guideline

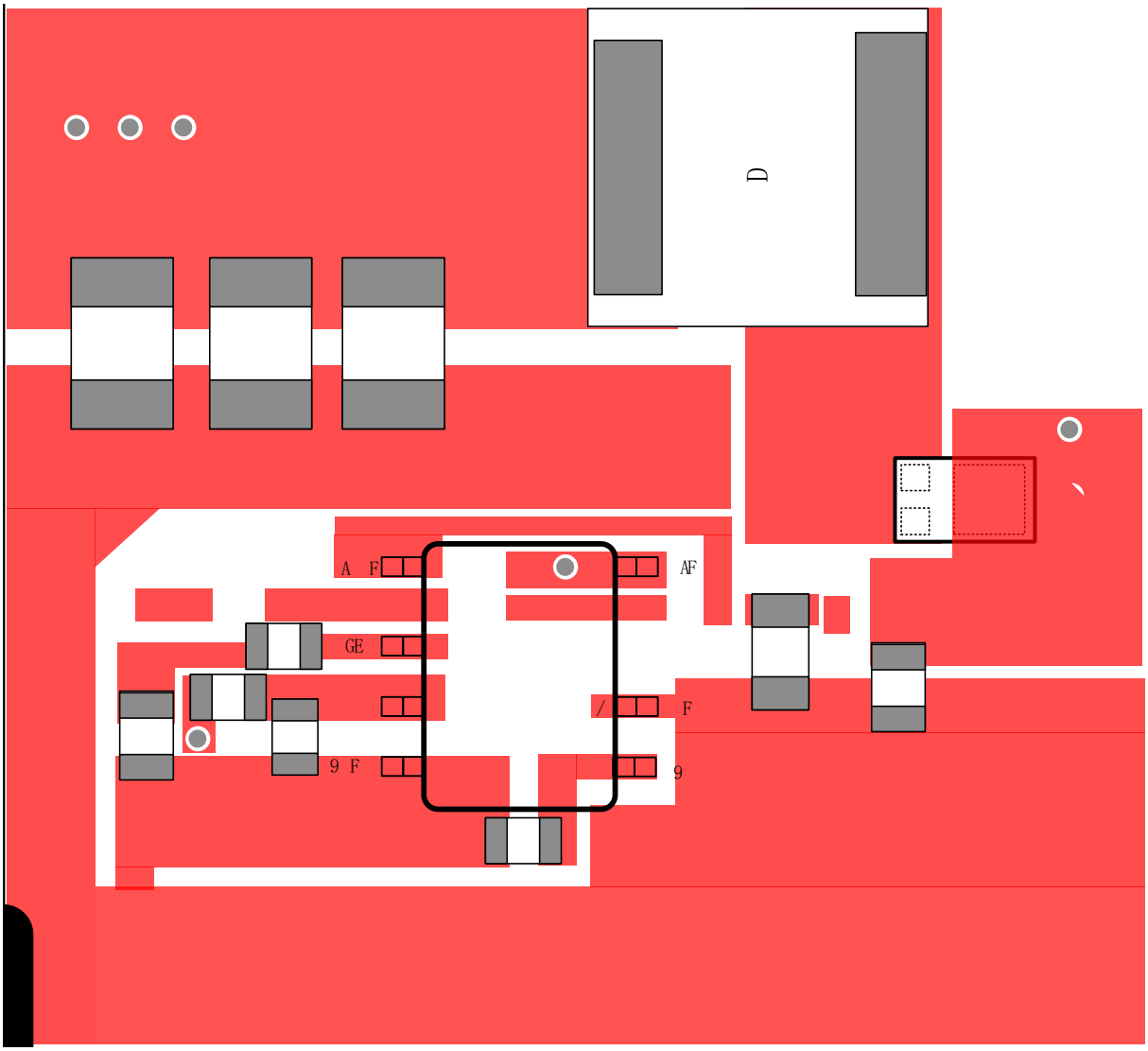

Figure 36. BOOST PCB Layout

NOTICE: The information in this document is subject to change without notice. Users should warrant and guarantee the third party Intellectual Property rights are not infringed upon when integrating Silicon Content Technology (SCT) products into any application. SCT will not assume any legal responsibility for any said applications.

