3.6V-36V Vin, 3A, High Efficiency Synchronous Step-down DCDC Converter

- Wide Input Range: 3.6V-36V
- Up to 3A Continuous Output Current
- 0.8V Feedback Reference Voltage
- Integrated 60mΩ High-Side and 36mΩ Low-Side Power MOSFETs
- Pulse Skipping Mode (PSM) with 30uA Quiescent Current in Sleep Mode
- 60ns Minimum On-time
- 4ms Internal Soft-start Time
- Adjustable Switching Frequency: 200k~2.2MHz
- Frequency Spread Spectrum (FSS) Modulation for EMI Reduction
- Precision Enable Threshold for adjustable Input Voltage Under-Voltage Lock Out Protection (UVLO) Threshold and Hysteresis
- Parallel input path to minimize switch node ringing
- Low Dropout Mode Operation
- Over-voltage and Over-Temperature Protection
- Available in 2mm*3mm QFN-12L Package

- Automotive infotainment and ADAS
- USB Type-C Power Delivery, USB Charging
- Industrial and Medical Distributed Power Supplies

The SCT2434D is 3A synchronous bu ý
age, ranging from 3.6V to 36V,

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.
Revision 0.8: Sample version.
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ORDERABLE DEVICE	PAC=AC	ϧ

PG	8	Open-drain power-good status output. Pull this pin up to a suitable voltage supply through a current limiting resistor. High = power OK, low = fault. PG output goes low when EN =low, VIN > 1V.
EN	9	Enable pin to regulator with internal pull-up current source. Pull below 1.12V to disable the converter. Float or connect to VIN to enable the converter. The t9

V_{IN}=24V, T_J=-40°C~125°C, typical value is tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
$t_{PGDFLT(rise}$	Delay time to PGOOD high signal			2		ms
$t_{PGDFLT(fall}$	Glitch filter time constant for PGOOD function			130		us
Protection						
V_{OVP}	Feedback overvoltage with respect to reference voltage	V_{FB}/V_{REF} rising		110		%
		V_{FB}/V_{REF} falling		105		%
V_{BOOTUV}		BOOT-SW falling		2.7		V
		Hysteresis		400		mV
T_{SD}	Thermal shutdown threshold*	T_J rising		160		°C
		Hysteresis		20		°C

*Derived from bench characterization

Figure 2. Efficiency, F_{SW}=400kHz, V_{OUT}=5V

Figure 3. Efficiency, F_{SW}=2.2MHz, V_{OUT}=5V

Figure 4. Line Regulation (FSW=400kHz,V_{OUT}=5V)

Figure 5. Input Current (V_{OUT}=5V, I_{LOAD}=0A)

Figure 6. Load Regulation (V_{IN}=12V, V_{OUT}=5V)

Figure 7

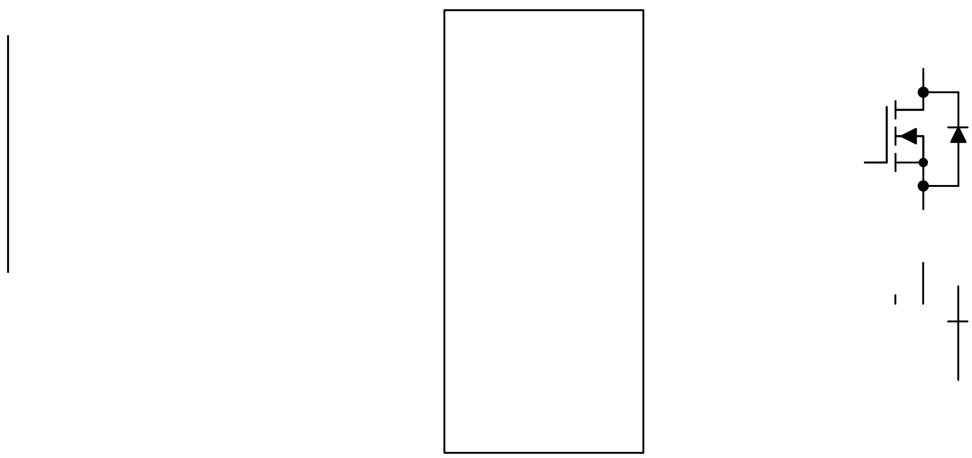

Figure 8. Functional Block Diagram

Overview

The SCT2434D is a 3.6V-36V input, 3A output, EMI friendly synchronous buck converter with built-in 60mΩ Rdson

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F_{SW}	R_6 (R_{FSW})
200 KHz	182 KΩ
300 KHz	120 KΩ
355 KHz	100 KΩ
400 KHz	88.7 KΩ
450 KHz	80.6 KΩ
520 KHz	68.1 KΩ
600 KHz	59 KΩ
700 KHz	51.1 KΩ

F_{SW}	R_6 (R_{FSW})
850 KHz	40.2 KΩ
1000 KHz	34.8 KΩ
1150 KHz	30.1 KΩ
1450 KHz	22.6 KΩ
1700 KHz	19.6

Figure 10. LDO Operation Characteristic (V_{OUT}=5V)

Over Current Limit and H

Typical Application

Output Voltage

The output voltage is set by an external resistor divider R_3 and R_4 in typical application schematic. When the output voltage is greater than 3V, recommended R_4 resistance is 24.9KΩ. Use Equation 4 to calculate R_3.

(4)

where:

(6)

where:

V_{rise} is rising threshold of Vin UVLO

V_{fall} is falling threshold of Vin UVLO

I_1=1uA, I_2=3.8uA, V_{ENR}=1.24V, V_{ENF}=1.12V

Inductor Selection

There are several factors should be considered in selecting inductor such as inductance, saturation current, the RMS current and

I_{LPP} is the inductor peak-to-peak current
I_{LRMS} is the inductor RMS current

In overloading or load transient conditions, the inductor peak current can increase up to the switch current limit of the device which is typically 4.5A. The most conservative approach is to choose an inductor with a saturation current rating greater than 4.5A. Because of the maximum I_{LPEAK} limited

The output ripple is essentially composed of two parts. One is caused by the inductor current ripple going through the Equivalent Series Resistance ESR of the output capacitors and the other is caused by the inductor current ripple charging and discharging the output capacitors. To achieve small output voltage ripple, choose a low-ESR output capacitor like

Application Waveforms

V_{IN}=12V, V_{OUT}=5V, unless otherwise noted

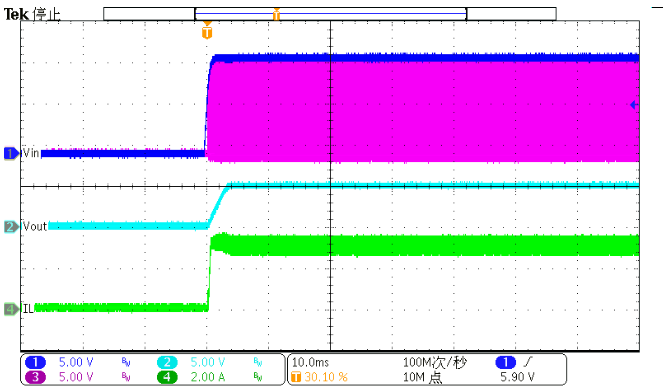


Figure 12. Power up(I_{LOAD}=3A)

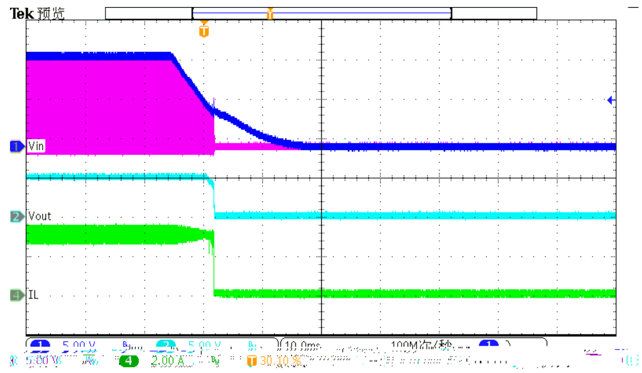


Figure 13. Power down(I_{LOAD}=3A)

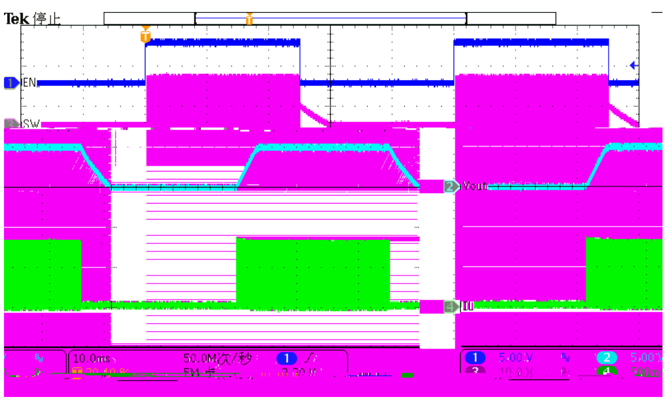


Figure 14. EN toggle (I_{LOAD}=0.1A)

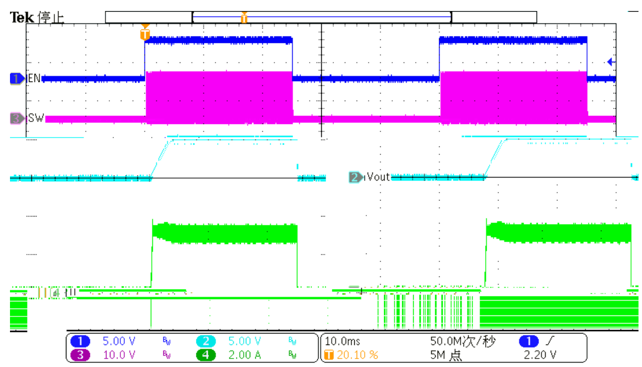


Figure 15. EN toggle (I_{LOAD}=3A)

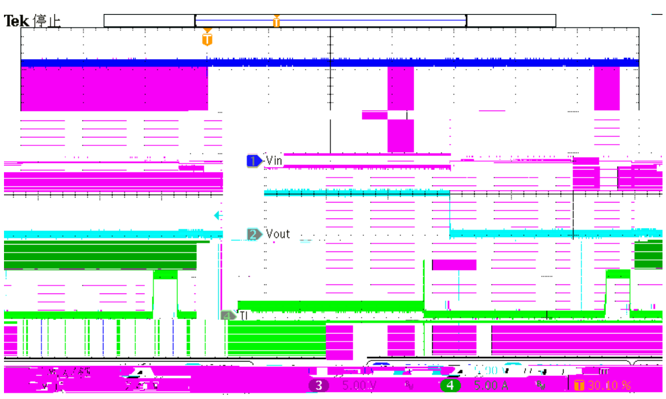


Figure 16. Over Current Protection(1A to hard short)

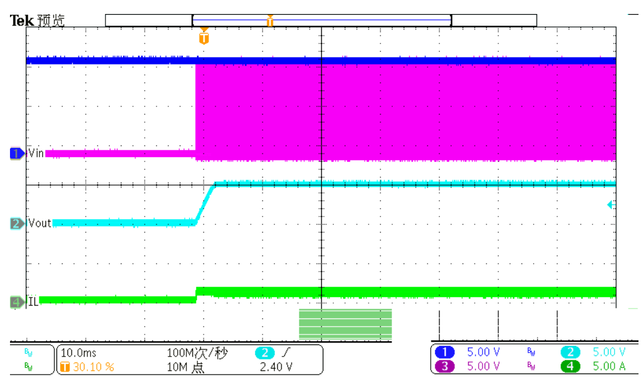


Figure 17. Over Current Release (hard short to 1A)

Application Waveforms

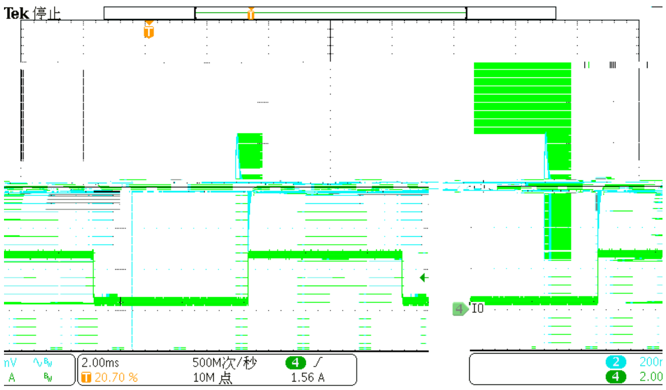


Figure 18. Load Transient (0.3A-2.7A, 1.6A/us)

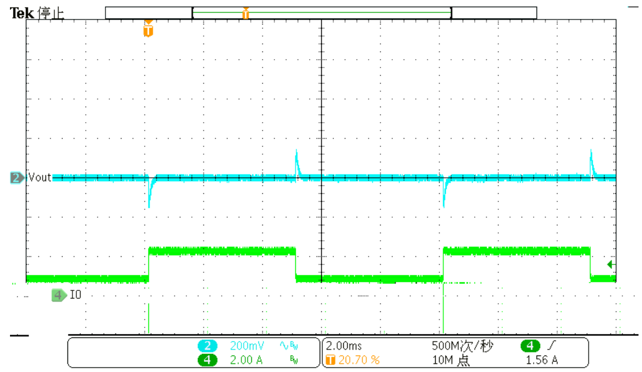


Figure 19. Load Transient (0.75A-2.25A, 1.6A/us)

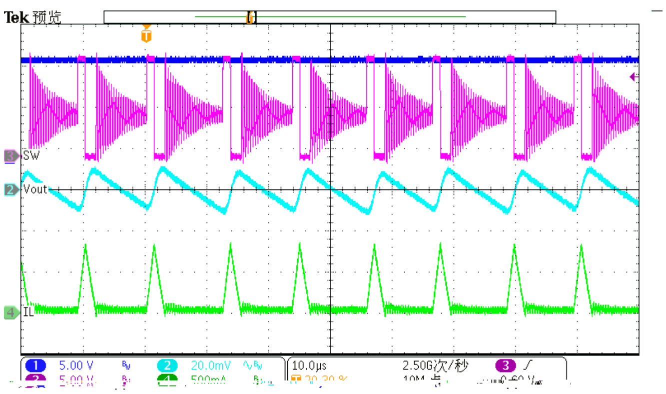


Figure 20. Output Ripple (I_{LOAD}=100mA)

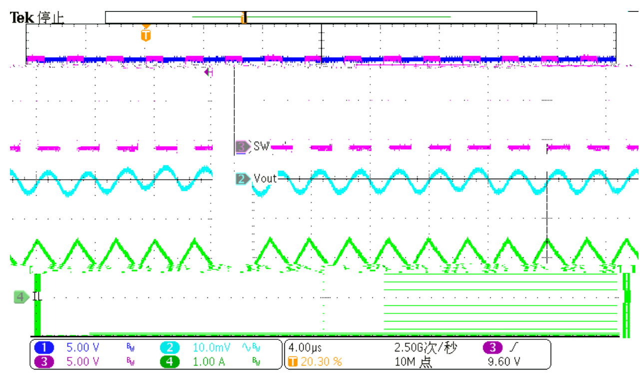


Figure 21. Output Ripple (I_{LOAD}=1A)

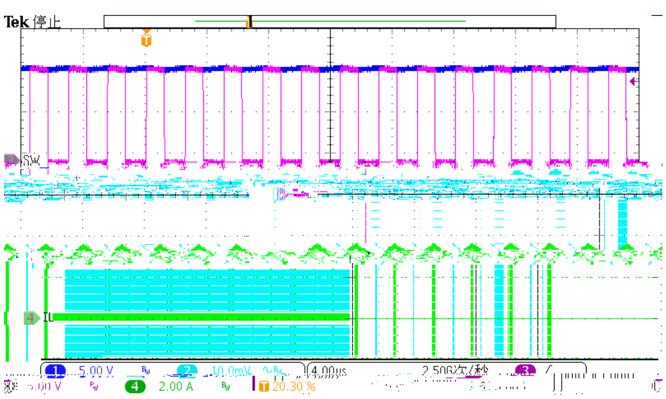


Figure 22. Output Ripple (I_{LOAD}=3A)

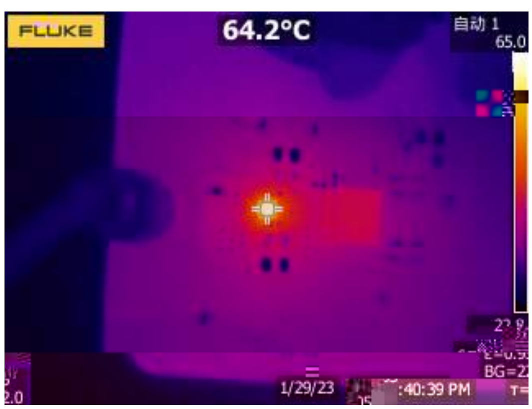


Figure 23. Thermal, 12V_{IN}, 5V_{OUT}, 3A

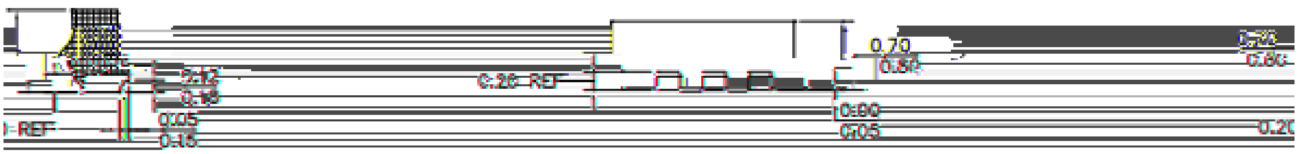
Layout Guideline

Proper PCB layout is a critical for SCT2434D’s stable and efficient operation. The traces conducting fast switching currents or voltages are easy to interact with stray inductance and parasitic capacitance to generate noise and degrade performance. For better results, follow these guidelines as below:

1. Power grounding scheme is very critical because of carrying power, thermal, and glitch/bouncing noise associated with clock frequency. The thumb of rule is to make ground trace lowest impendence and power are distributed evenly on PCB. Sufficiently placing ground area will optimize thermal and not causi [illegible]

BOTTOM VIEW

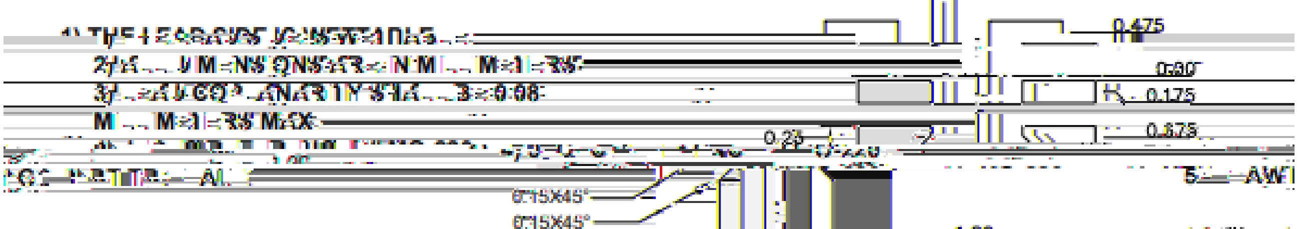
TOP VIEW

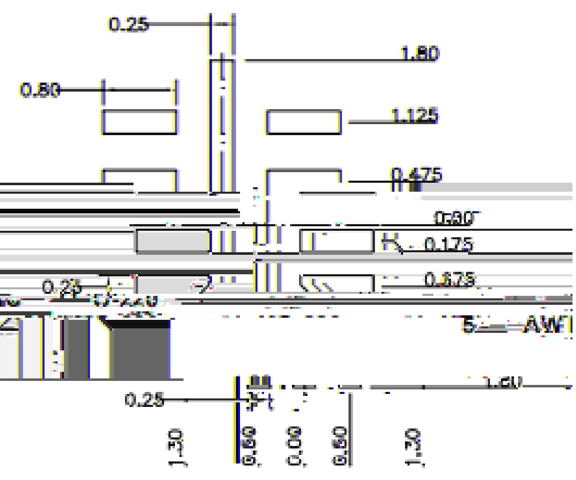


SECTION A-A

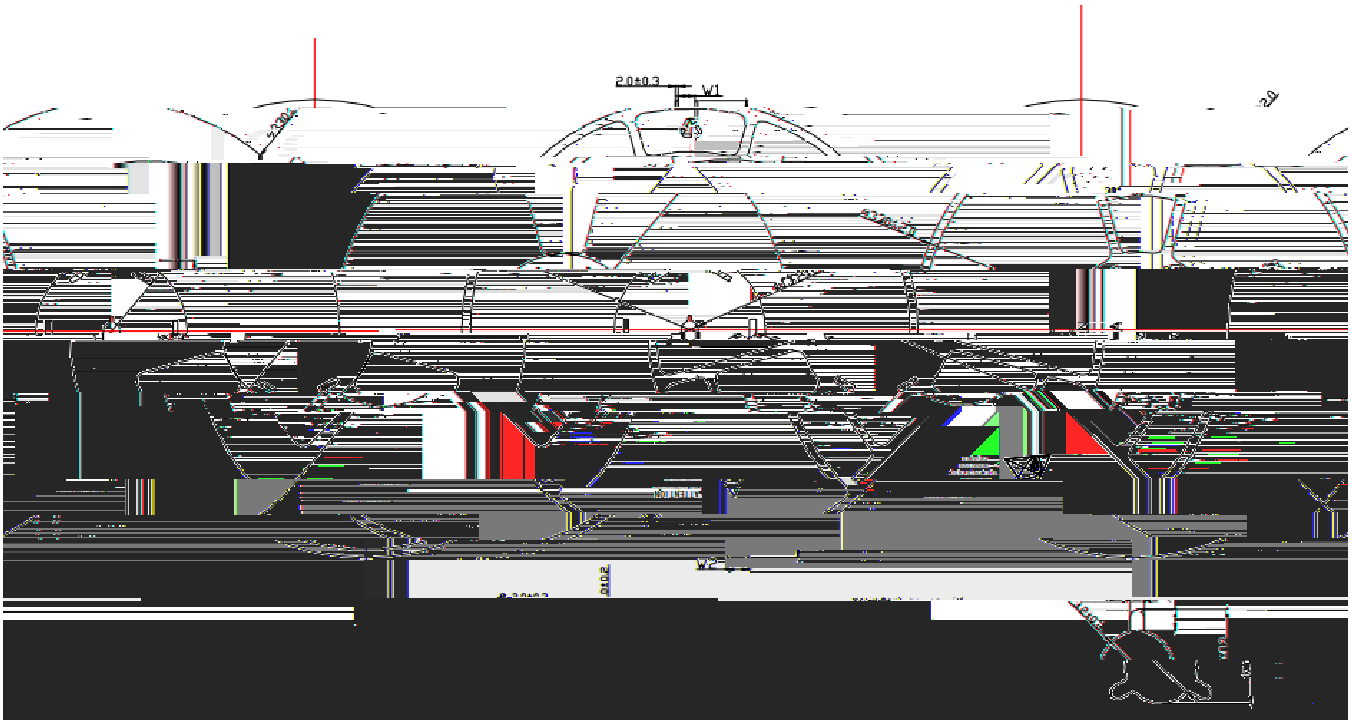
SIDE VIEW

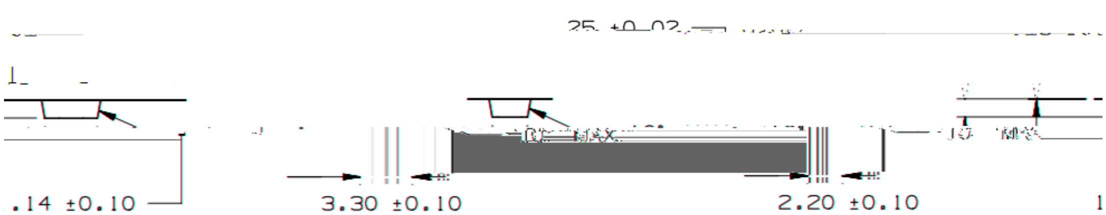
NOTE:





RECOMMENDED LAND PATTERN




3.30 ±0.10
2.20 ±0.10

