12V, 7A Fully Integrated High Efficiency Synchronous Boost Converter

FEATURES

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REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision 1.0:

ELECTRICAL CHARACTERISTICS

V_{IN}=3.6V, T_J=-40℃~125℃, typical values are tested under 25℃.

V_{IN}	Operating input voltage		2.75	

TYPICAL CHARACTERISTICS

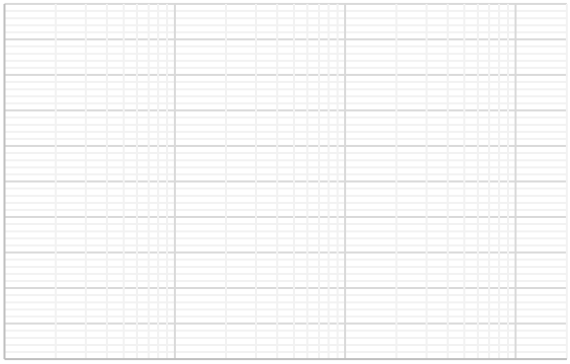


Figure 1. SCT1270Q Efficiency vs Load Current, Vout=9V

Figure 2. SCT1270Q Efficiency vs Load Current, Vin=3.6V

Figure 3. Load Regulation (Vin=3.6V, Vout=9V)

Figure 4. Line Regulation, Vout=9V

Figure 5. Current Limit VS Setting Resistance

Figure 6. Switching Frequency VS Setting Resistance

(minimum 0.4V). An internal 750kΩ resistor connects EN pin to the ground. Floating EN pin automatically disables the device.

The SCT1270Q features fixed 4ms soft start to prevent inrush current during power-up.

The SCT1270Q boost converter implements cycle-by-cycle peak current limit function with sensing the internal low-side power MOSFET Q1 during overcurrent condition. While the Q1 is turned on, its conduction current is monitored by the internal sensing circuitry. Once the low-side MOSFET Q1 current exceeds the limit, it turns off immediately. An external resistor connecting ILIM pin to ground sets the low-side MOSFET Q1 peak current limit threshold. Use Equation 1 or Figure 5 to calculate the peak current limit.

$$\frac{\quad}{\quad} \tag{1}$$

where:

- I_{LIM} is the peak current limit
- R_{LIM} is the resistance between ILIM pin to ground.

This current limit function is realized by detecting the current flowing through the low-side MOSFET. The current limit feature loses function in the output hard short circuit conditions. At normal operation, when the output hard shorts to ground, there is a direct path to short the input voltage through high-side MOSFET Q2 or its body diode even the Q2 is turned off. This could damage the circuit components and cause catastrophic failure at load circuit.

The SCT1270Q

and reaches a threshold with respect to the peak current of I_{LIM} / 10, the output of the error amplifier is clamped at this value and does not decrease any more. If the load current is smaller than what the SCT1270Q delivers, the output voltage increases above the nominal setting output voltage. The SCT1270Q extends its off time of the switching period to deliver less energy to the output and regulate the output voltage to 1.0% higher than the nominal setting voltage. With the PFM operation mode, the SCT1270Q keeps the efficiency above 70% even when the load current decreases to 1 mA. At light load, the output voltage ripple is much smaller due to low peak inductor current. Refer to Figure 17.

Once the junction temperature in the SCT1270Q exceeds 164 ℃, the thermal sensing circuit stops switching until the junction temperature falling below 140 ℃, and the device restarts. Thermal shutdown prevents the damage on device during excessive heat and power dissipation condition.

The performance of inductor affects the power supply's steady state operation, transient behavior, loop stability, and boost converter efficiency. The previous calculations and bench evaluation. In this application, the Wurth-Elektronix 's inductor 744313220 is used 73.549(du)4(c)-5(to on SCT1270Q evaluation board.

744325180	1.8	3.5	18 / 14	10.5 x 10.2 x 4.7	Wurth Elektronix
744311150	1.5	7.2	14 / 11	7.3 x 7.2 x 4.0	Wurth Elektronix
744311220	2.2	12.5	13 / 9	7.3 x 7.2 x 4.0	Wurth Elektronix
744313220	2.2	5.7	18 / 14	12.9 x 12.8 x 3.3	Wurth Elektronix
CDMC8D28NP-1R8MC	1.8	12.6	9.4 / 9.3	9.5 x 8.7 x 3.0	Sumida

For good input voltage filtering, choose low-ESR ceramic capacitors. A 0.1μF ceramic bypass capacitor is recommended to be placed as close as possible to the VIN pin of the SCT1270Q. A ceramic capacitor of more than 1.0μF is required at the VCC pin to get a stable operation of the internal LDO.

For the power stage, because of the inductor current ripple, the input volt

An external loop compensation network comprises resister R5, ceramic capacitors C5 and C6 connected to the COMP pin to optimize the loop response of the converter. The power stage small signal loop response of constant off time with peak current control can be modeled by equation 11.

Vin=3.6V, Vout=9V, unless otherwise noted

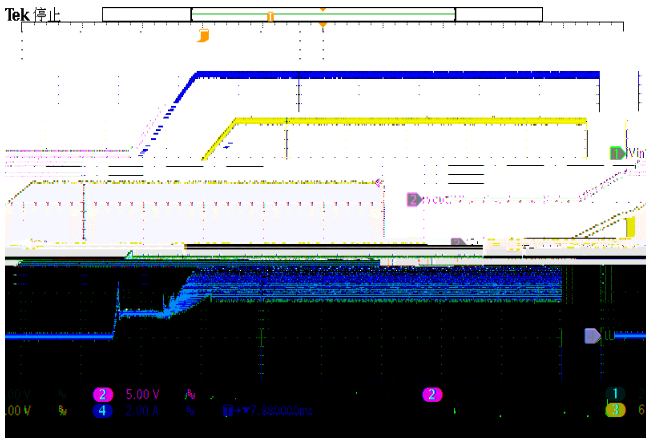


Figure 9. Power up

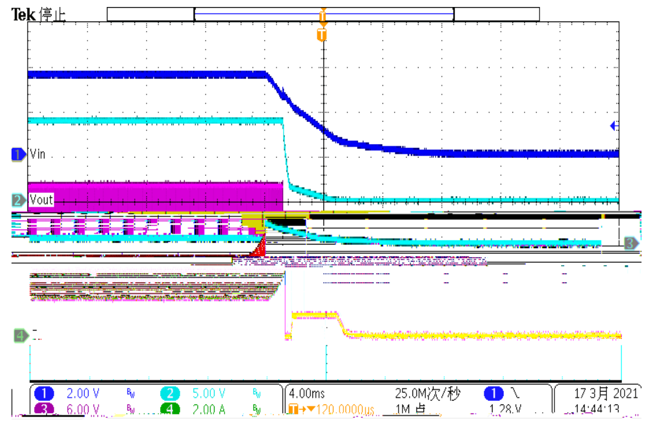


Figure 10. Power down

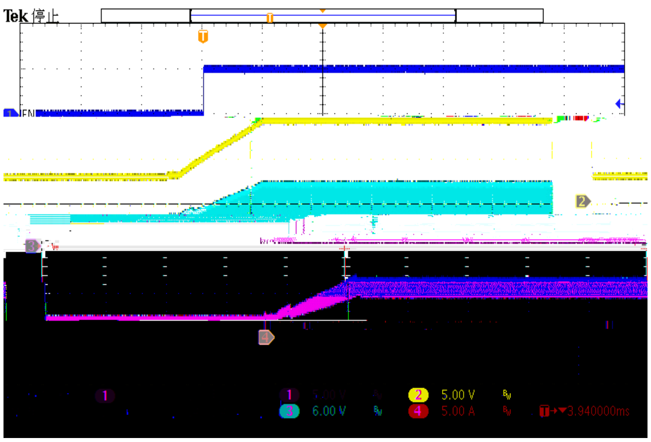


Figure 11. EN Power up (Iload=2A)

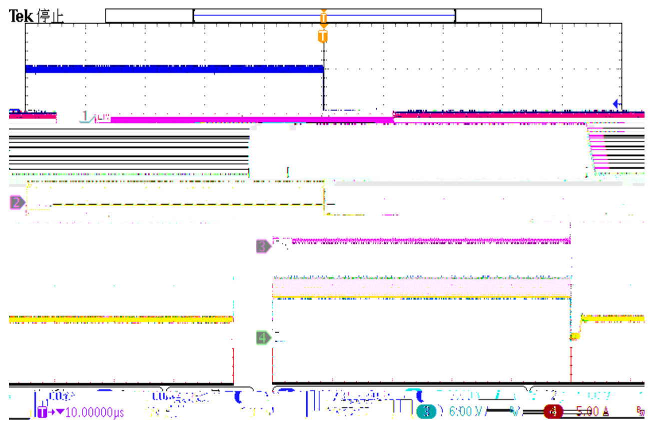


Figure 12. EN Power down (2A)

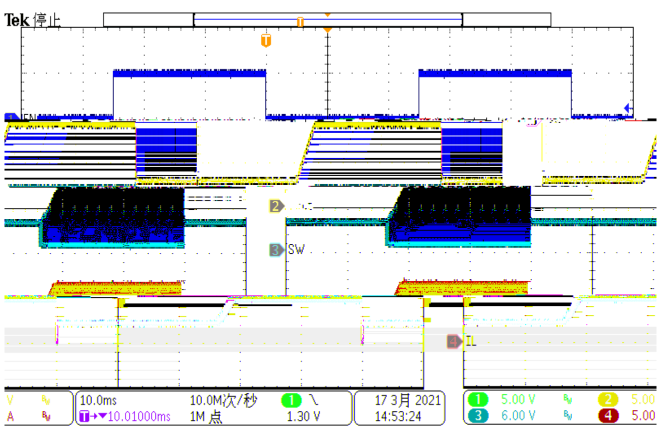


Figure 13. EN toggle (Iload=2A)

Figure 14. EN toggle (Iload=10mA)

Vin=3.6V, Vout=9V, unless otherwise noted

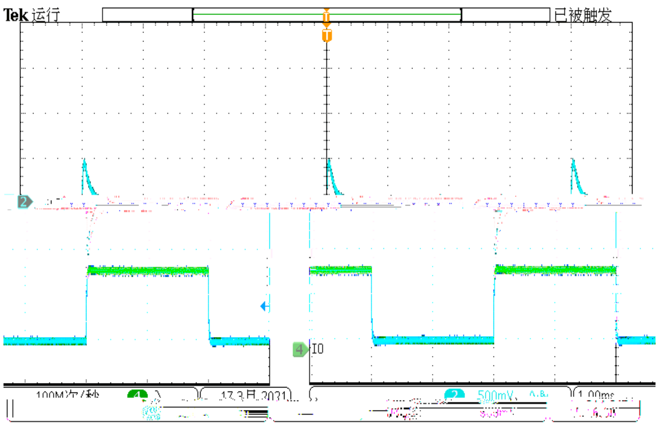


Figure 15. Load transient (0.2A-1.8A, 1.6A/us)

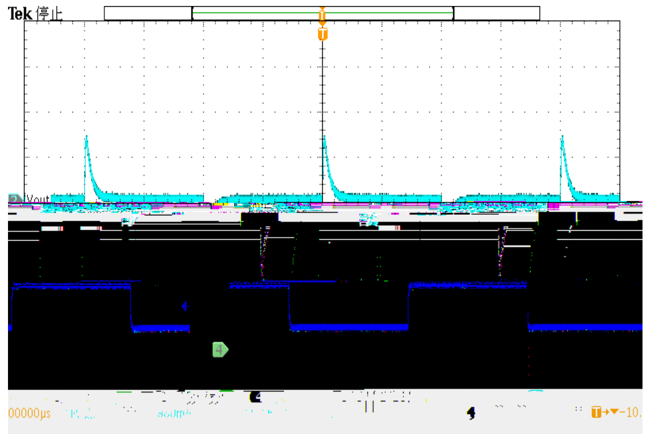


Figure 16. Load transient (0.5A-1.25A, 1.6A/us)

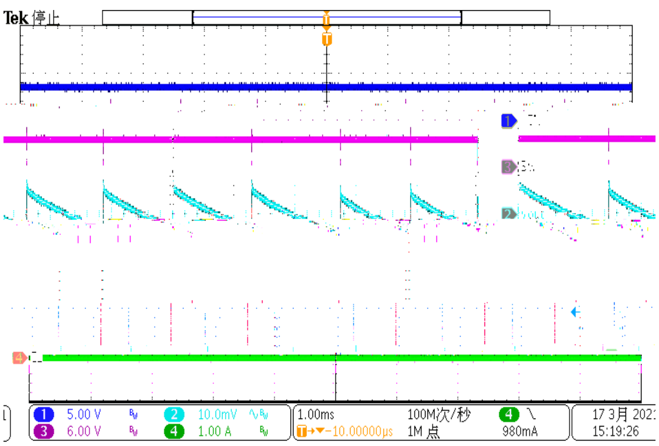


Figure 17. Steady state (Iload=0A, PFM)

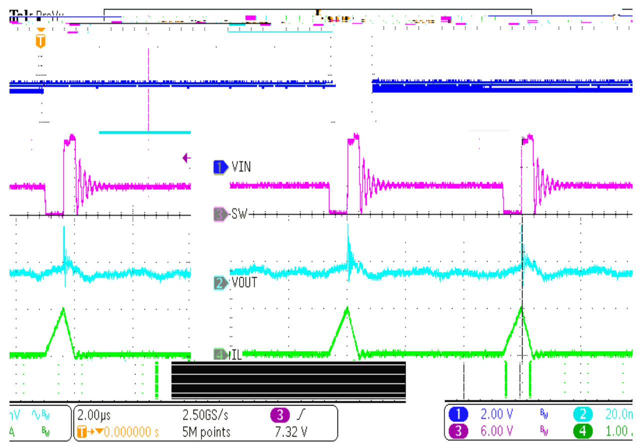


Figure 18. Steady state (Iload=30mA, PFM)

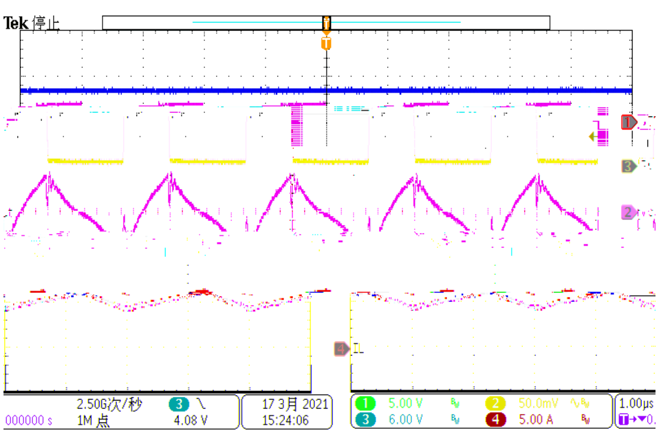


Figure 19. Steady state (Iload=2A)

Figure 20. Thermal, Vin=3.6V, Vout=9V, Iload=2A

The regulator could suffer from instability and noise problems without careful layout of PCB. Radiation of high-frequency noise induces EMI, so proper layout of the high-frequency switching path is essential. Minimize the length and area of all traces connected to the SW pin, and always use a ground plane under the switching regulator to minimize coupling. The input capacitor needs to be close to the VIN pin and ground pad to reduce the input supply ripple.

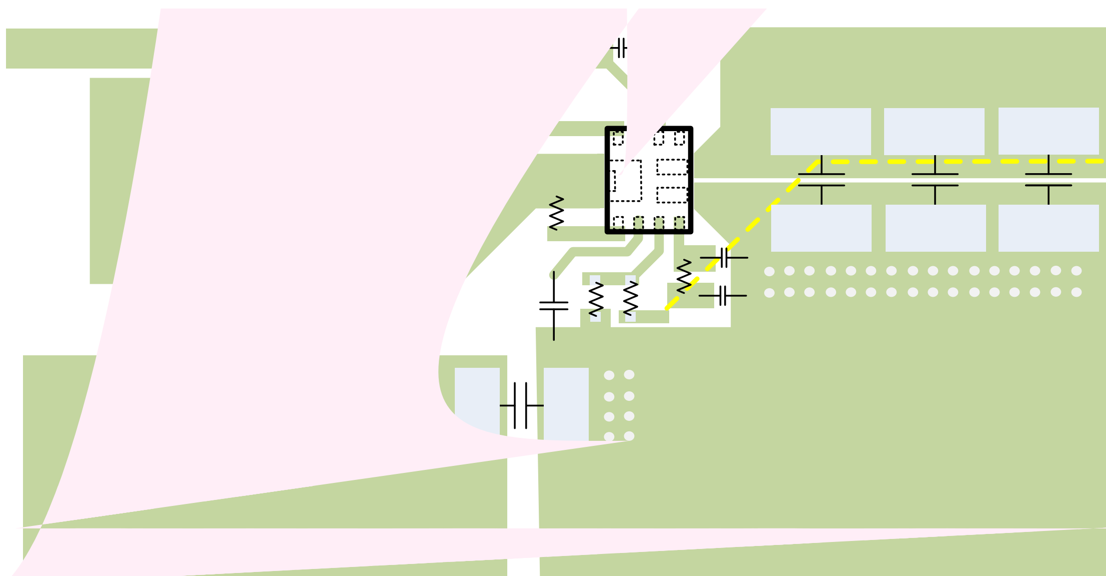
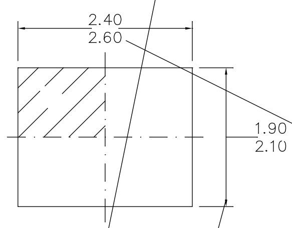
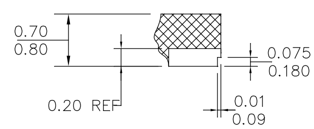


Figure 21. PCB Layout Example Top Layer

PACKAGE INFORMATION





TAPE AND REEL INFORMATION