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The SCT2113M is a 2.65V-5.5V input, 0.6A output, synchronous buck converter with built-in MOSFETs and inductor. It implements constant on time control to regulate output voltage, providing excellent line and load transient response.

The switching frequency is fixed 2.2MHz. The SCT2113M features integrated soft start time to avoid large inrush current and output voltage overshoot during startup. The SCT2113M operates in Pulse Frequency Modulation (

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The output voltage is set by an external resistor divider R1 and R2 in typical application schematic. Recommended R2 resistance is 10.2kΩ. Use Equation 4 to calculate R1.

$$_1 = (\text{——} - 1) \quad _2 \qquad (4)$$

where:

- V_{REF} is the feedback reference voltage, typical 0.6V

1.2 V	10.2 kΩ	10.2 kΩ
1.8 V	20 kΩ	10.2 kΩ
2.5V	32.4 kΩ	10.2 kΩ
3.3 V	68 kΩ	15 kΩ

The input current to the step-down DCDC converter is discontinuous, therefore it requires a capacitor to supply the AC current to the step-down DCDC converter while maintaining the DC input voltage. Use capacitors with low ESR for better performance. Ceramic capacitors with X5R or X7R dielectrics are usually suggested because of their low ESR and small temperature coefficients, and it is strongly recommended to use another lower value capacitor (e.g., 0.1uF) with small package size (0603) to filter high frequency switching noise. Place the small size capacitor as close to VIN and GND pins as possible.

The voltage rating of the input capacitor must be greater than the maximum input voltage. And the capacitor must also have a ripple current rating greater than the maximum input current ripple. The RMS current in the input capacitor can be calculated using Equation 5.

$$I_{CINRMS} = I_{OUT} \sqrt{\frac{V_{OUT}}{V_{IN}} (1 - \frac{V_{OUT}}{V_{IN}})} \qquad (5)$$

The worst case condition occurs at $V_{IN}=2*V_{OUT}$, where:

$$I_{CINRMS} = 0.5 \quad I_{OUT} \qquad (6)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

When selecting ceramic capacitors, it needs to consider the effective value of a capacitor decreasing as the DC bias voltage across a capacitor increasing.

The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated usin 6.96 Tf1 0 0 1 315.89 363.53 t.96 Tf1 0 0 1 315.89 363.53 t.96 Tf1 0 0 1 315.89 363.53 89 363US

For this example, 22μF, X7R ceramic capacitors rated for 16 V in parallel are used. And a 0.1μF for high-frequency filtering capacitor is placed as close as possible to the device pins.

The selection of output capacitor will affect output voltage ripple in steady state and load transient performance.

The output ripple is essentially composed of two parts. One is caused by the inductor current ripple going through the Equivalent Series Resistance ESR of the output capacitors and the other is caused by the inductor current ripple charging and discharging the output capacitors. To achieve small output voltage ripple, choose a low-ESR output capacitor like ceramic capacitor. For ceramic capacitors, the capacitance dominates the output ripple. For simplification, the output voltage ripple can be estimated by Equation 8 desired.

$$\Delta V_{OUT} = \frac{(\quad - \quad)}{8 \quad ^2} \qquad (8)$$

Where:

- ΔV_{OUT} is the output voltage ripple.
- f_{SW} is the switching frequency.

