REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version

Revision 1.0: Released to Market

Revision 1.1: Update DEVICE ORDER INFORMATION

Revision 1.2: Corrected few typographical errors.

Revision 1.3: Update DEVICE ORDER INFORMATION.

DEVICE ORDER INFORMATION

PART NUMBER	PACKAGING TYPE

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PIN FUNCTIONS (continued)

NAME	NO.	DESCRIPTION

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THERMAL INFORMATION(continued)

PARAMETER	THERMAL METRIC	QFN-18L	UNIT
R -&(top)	Junction to case (top) thermal resistance(1)	46.8	°C/W
R -B	Junction to board thermal resistance(1)	8.8	

(1) SCT provides R -$and R -&numbers only as reference to estimate junction temperatures of the devices. R -$and R -&are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT61240 is mounted, thermal pad size, and external environmental factors. The PCB board is a heat sink that is soldered to the leads and thermal pad of the SCT61240. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual R -$and R -&

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ELECTRICAL CHARACTERISTICS

V_{IN}=10V, T_A=-40°C~150°C, typical values are tested under 25°C.

SYMBOL	PARAMETER

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ELECTRICAL CHARACTERISTICS (Continued)

V_{IN}=10V, T_A=-40°C~150°C, typical values are tested under 25°C

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
BUCK2 (LV BUCK)						
V_{IN23}	VIN23 Input Voltage Range		2.7		5	V
V_{OUT2}	VOUT2 Output Voltage			1.8		V
V_{OUT2_ACC}	VOUT2 Accuracy		-2		2	%
$R_{DS_H_BK2}$	High-side MOSFET on-resistance	V_{OUT1}=3.1V		155	260	m Ÿ
$R_{DS_L_BK2}$	Low-side MOSFET on-resistance	VIN>5V		75	125	m Ÿ
$I_{ILEAK_HS_BUCK2}$	SW2 HS Switch Leakage Current	T_A=25°C		0.01	1	A
		T_A=-40°C~150°C		7		A
$I_{ILEAK_LS_BUCK2}$	SW2 LS Switch Leakage Current			0.01	1	A
I_{PEAK_BUCK2}	Peak Current Limit		0.9	1.2	1.65	A
I_{VALLEY_BUCK2}	Valley Current Limit		0.65	1	1.3	A

/ACLE(f)20 0 Tw 0 -0 0.9 168.8 Tm [(MC (ÿ< <MCID 121>>BDC 206.857 0 Td3 47-2 (.9 /P <</MCID 122 >>BDC 207.853 0 T0.015 Tw 2.553 0 T0A947-2 (.9 75EMC 1.28 0 Td 1A1)Tj 2.00 /P <</MCID 122

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ELECTRICAL CHARACTERISTICS (Continued)

V_{IN}=10V, T_A=-40°C~150°C, typical values are tested under 25°C.

SYMBOL	PARAMETER

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.silicon.core.fabrication 728.16 728.16 140 0c 0 0w 9.01509 TdT 8.04 0 Q 409 TdT 8.04 -0.000 0c 0.01C w0 1Q 409 TdT[(©)1.7 (Tm 24)14.

TYPICAL CHARACTERISTICS (continued)

V_{IN}=10V, T_A=-40°C~125°C, unless otherwise noted.

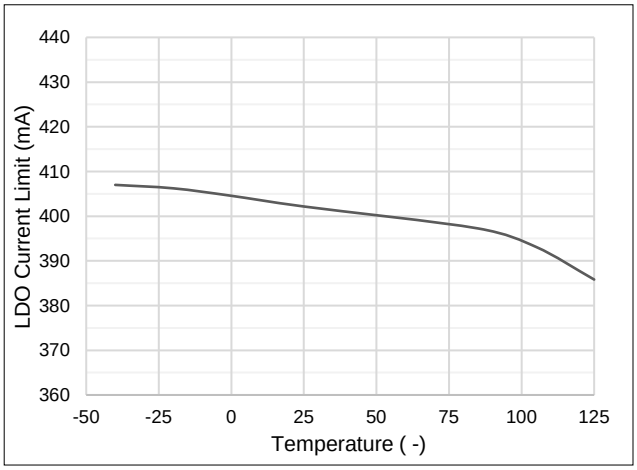

Figure 7. LDO Current Limit vs. Temperature

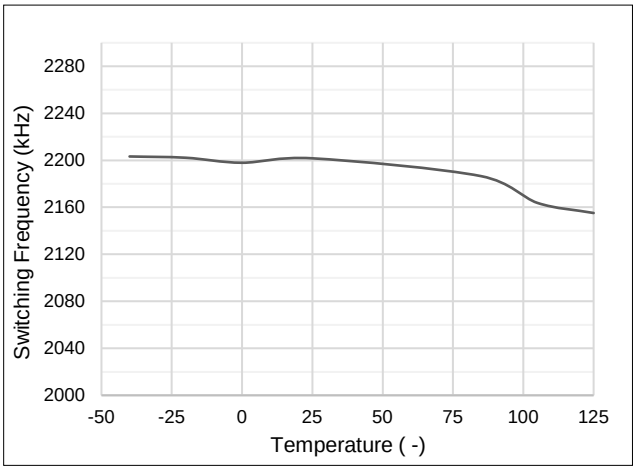

Figure 8. Switching Frequency vs. Temperature

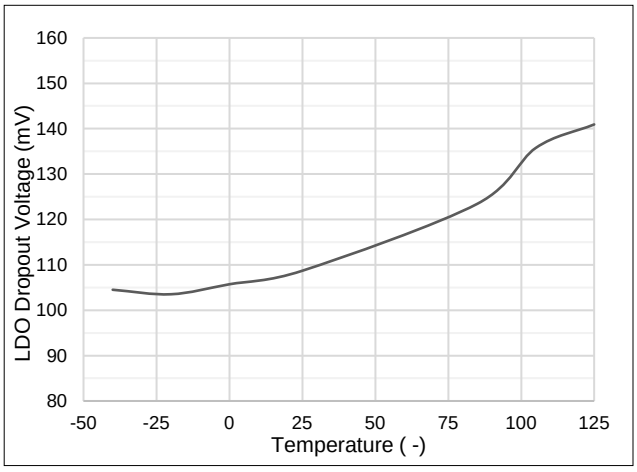

Figure 9. LDO Dropout Voltage vs. Temperature, ILDO=300mA

Figure 10. LDO PSRR, ILDO=100mA

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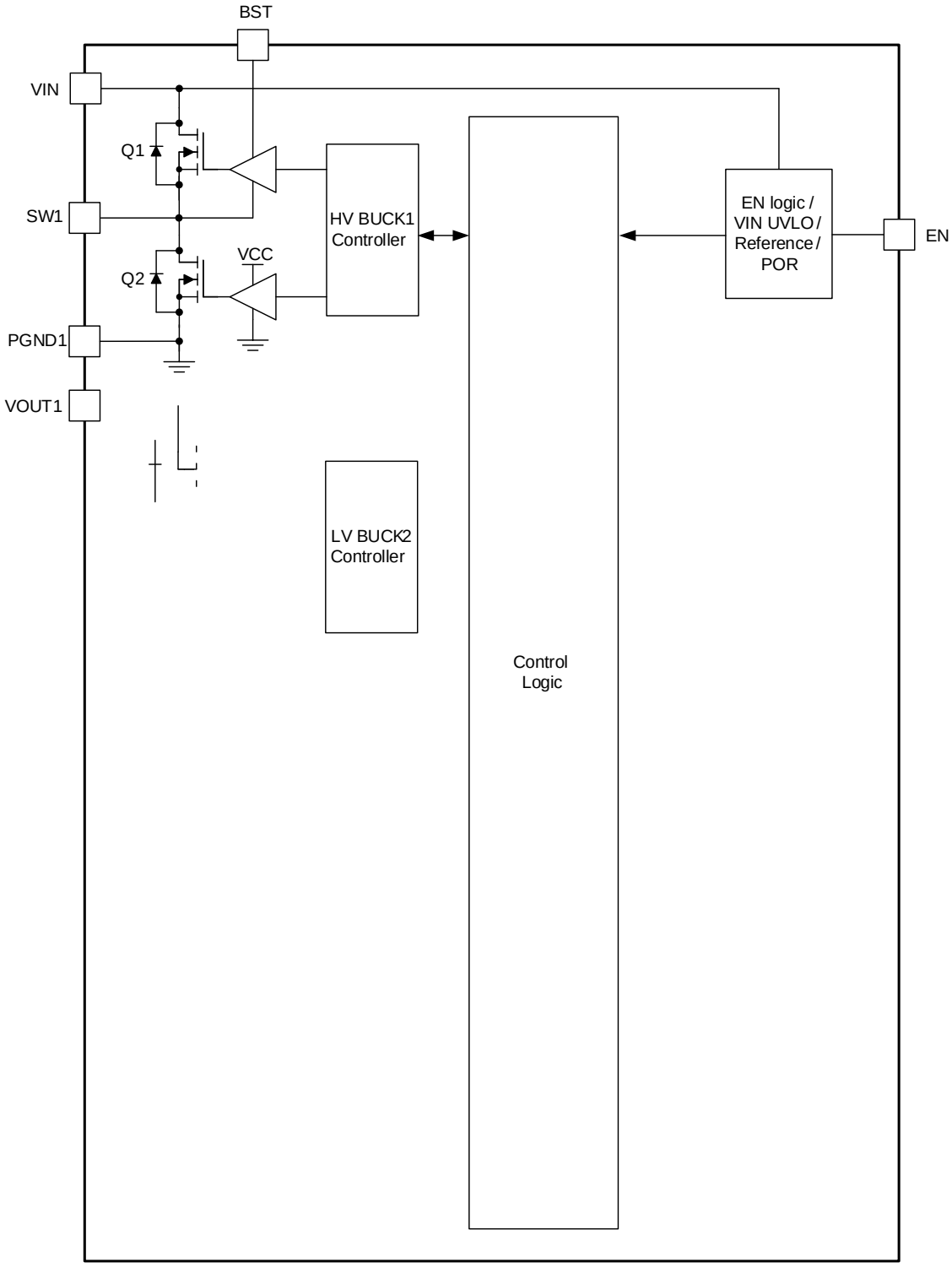
FUNCTIONAL BLOCK DIAGRAM



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OPERATION

Overview

The SCT61240 is a highly integrated power management IC (PMIC) optimized for camera system. It integrates three high efficiency synchronous BUCK converters (HVBUCK1, LVBUCK2, LVBUCK3), and a high-PSRR low noise LDO with OV/UV monitoring on all outputs.

VOUT1 is the output of BUCK1, which is powered from VIN (Power Over Coax) and can output 1.2A continuous current with the output voltage set to LDOOUT+300mV/500mV or fixed 3.3V.

VOUT2 is the output of BUCK2, which is powered from VOUT1 and can output 600mA continuous current with the output voltage fixed to 1.8V.

VOUT3 is the output of BUCK3, which is powered from VOUT1 and caicr1.2 ( )0.7 (3 (t)-1.1 1.)-1.1 (2)-12.2 (9 (V)2.3 (m( )0 oop-1.1 (h)-12.3 rt volV -op-11.1(h)-11be(ut)-1.1.1 (s)-8 (r)2.3 (uou2)-8.1 ( )]TJ 0.0011xed11.r()-12.3 (V)-9.72.627 cage (c)-8 oop-19 (n (i)3.1 (oea(-op-11.1ur)-63 (n)(s)-8 (pna-12.2(h)lnt)21. 51.)-1.1 e1)ns(s)-8 (pe1)nh op (t)-1.y.18 (r)2.3 (uou2)-8.[2a(u

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Under Voltage Protection

If an output falls below the under voltage protection threshold, all outputs will shut off for the hiccup time. When hiccup ends, the normal power up sequence will start again according to the SEQ and RSET setting. When entry hiccup, the output discharge will operate during the hiccup time.

Over Current Protection (OCP)

For the three bucks and LDO, the SCT61240 provides both peak and valley current limit designed to limit the peak/valley inductor current to ensure that the switching currents remain within the device capabilities during overload conditions or during an output short circuit.

When the HS-FET turns on, the chip monitors the increased IL through the relevant operating main power switch. Once the peak IL exceeds the peak current limit threshold, the HS-FET turns off immediately, and the LS-FET turns on to conduct and decrease IL. The HS-FET does not turn on again until IL falls below the valley current limit threshold.

Power Good

The PG pin is a push-pull output. It goes to logic high when the device is powered on, and all outputs are within the power good range, and no faults reported. The high output level can be programmed to either 3.3V or 1.8V.

PG will assert low when any of below events occur:

- Buck1's output is out of power good range or VOUT OV/UV range
- Buck2's output is out of power good range or VOUT OV/UV range
- Buck3's output is out of power good range or VOUT OV/UV range
- LDO's output is out of power good range or VOUT OV/UV range
- Junction temperature is over Thermal Shutdown point
- VIN is higher than VIN OVP threshold

Hiccup or L atch off P rotection

When below faults are detected, the SCT61240 will enter hiccup or latch off mode (programmable option). When select hiccup mode and entry hiccup, all the channels shut off for 3.6ms, and then the normal power up sequence will start again according to the SEQ and RSET setting. When select latch off mode and entry latch off, all the channels shut off and not restart unless VIN/EN power on reset (POR).

The faults that make the device entry hiccup/latch off protection:

- Buck1's output is out of VOUT OV/UV range
- Buck2's output is out of VOUT OV/UV range
- Buck3's output is out of VOUT OV/UV range
- LDO's output is out of VOUT OV/UV range
- Junction temperature is over Thermal Shutdown point
- VIN is higher than VIN OVP threshold

Output Discharge

In order to discharge the energy of output capacitor during power off sequence, all channels have active discharge path from their output to ground. The discharge path is turn-on when channel is disabled.

Internal Soft- Start

The soft start function is implemented to prevent the PMIC output voltage from overshooting during start Vu (ut)-1.1(T)-5.4 Wti

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Frequency Spread Spectrum

To meet CISPR and EMI compliances, the SCT61240 implements Frequency Spread Spectrum (FSS) function. The FSS circuitry shifts the 2.2MHz switching frequency within ±5% range and 1/512 of the switching frequency periodically. Therefore, the SCT61240 can guarantee that the switching frequency does not drop into the 1.8MHz AM band limit.

Thermal Shutdown

The SCT61240 protects the device from damage during excessive heat and power dissipation condition. Once the junction temperature exceeds 170C, the thermal sensing circuit disable all channels and enter hiccup or latch off. When the junction temperature falls below 150C and hiccup ends, then the device restarts.

Power on/off S equence Control

For power on, the SCT61240 supports 6 power-on sequences for buck2&3 and LDO through SEQ pin. Since the output of BUCK1 is the power for the next three channels, BUCK1 is always set to startup first.

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Figure 12. Example SEQ1 for SCT61240

Output Voltage Setting

The device provides 9 flexible voltage setting through RSET PIN for various sensors. Connect a resistor between RSET and GND to set the output voltage of each channel before enabling the device. The RSET detection only activated at the beginning of power on, and the output voltage configuration is latched once RSET detection done. Any change during the power on procedure is not guarantee to the correct output voltage setting.

Below table shows the output voltage setting with its corresponding resistance.

Table 2. Output Voltage Setting

RSET No.	RSET Resistance(			Output voltage(V)				
	MIN	TYP	MAX	BUCK1 (SCT61240-0000)	BUCK1 (SCT61240-0001)	BUCK2	BUCK3	LDO
VSET1	0	0						

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- $V_{IN(max)}$ is the maximum input voltage
- $I_{OUT(max)}$ is the maximum DC load current
- LIR is coefficient of I_{LPP} to I_{OUT}

The total current flowing through the inductor is the inductor ripple(t)-1.1 (or)-6.4 (r)-6.3 (i)3.1 (pi2or)-6.4 (r)-6.3 (i)3.1 (ppl)-8.9
l ti ot55.7 (i)9.1he (i)3(m)2(i)c 810ho (i)3.1 (, (h(or)-4 (r)-6.3 (i)c 39 (Td [8)-peak.3 (d)2.3 (dough t)-13.2 (he (r)-6. t)-1.h13.2 (h

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Application Waveforms

Vin=10V, RSET=SEQ=8kq\, V_{OUT1}=3.0V, V_{OUT2}=1.8V, V_{OUT3}=1.2V, V_{OUT4}=2.7V,unless otherwise noted

Figure 15. Power On (Io2=0.6A, Io3=1.2A, Io4=0.3A)

Figure 16. Power Off (Io2=0.6A, Io3=1.2A, Io4=0.3A)

Figure 17. EN On (Io2=0.6A, Io3=1.2A, Io4=0.3A)

Figure 18. EN Off (Io2=0.6A, Io3=1.2A, Io4=0.3A)

Figure 19. Buck1 Over Current Protection
(1.2A to hard short)

Figure 20. Buck1 Over Current Release
(hard short to 1.2A)

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Application Waveforms (continued)

Vin=10V, RSET=SEQ=8kq\, V_{OUT1}=3.0V, V_{OUT2}=1.8V, V_{OUT3}=1.2V,EQ=8kOUT3A4004 Tc 0.004 Tw 9.96 -0 0 9.96 260.04 312 T

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Layout Guideline

Proper PCB layout is a critical for SCT61240's stable and efficient operation. The traces conducting fast switching currents or voltages are easy to interact with stray inductance and parasitic capacitance to generate noise and degrade performance. For better results, follow these guidelines as below:

1. Power grounding scheme is very critical because of carrying power, thermal, and glitch/bouncing noise associated with clock frequency. The thumb of rule is to make ground trace lowest impendence and power are distributed evenly on PCB. Sufficiently placing ground area will optimize thermal and not causing over heat area.

2. Place a low ESR ceramic capacitor as close to VIN pin and the ground as possible to reduce parasitic effect.

3. For operation at full rated load, the top side ground area must provide adequate heat dissipating area. Make sure top s.2 (n)-14 0 Td [0e-8.9 (oo94)21 0 Td (ng)-12.3 (no)-1 (y)-8 (o (un)-12.p 14 0 Td [0e-8.9 (oo94)21h(a)-12.p (er)-6.3

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PACKAGE INFORMATION

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TAPE AND REEL INFORMATION

Type	$A_0^{+0.1}$ mm	Carrier Width	Diameter
PRA ; F4DK	9.3	12	B=76.2±0.10mm C=92.2±0.25mm
HST	9.5	12	
HST	13.5	16	
HST ; C800	21.3	24	
2420S	13.3	16	
2420S	21.3	24	
TIST300	9.9	12	

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Symbol	Dimensions in Millimeters
A0	2.75±0.10
B0	3.75±0.10
D	$1.5^{+0.10}$
D1	1.00±0.10
E	1.75±0.10
F	5.50±0.05
K0	1.00±0.10
P	4.00±0.10
P0	4.00±0.10
P2	2.00±0.05
t	0.25±0.03
W	$12.00^{+0.30}_{-0.10}$
	5° max

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