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| NAME | NO. | DESCRIPTION |
|---|---|---|
| VOUT1 | 14 | Voltage sense for the output of Buck1. The device regulates VOUT1 voltage to the setting value. The device regulates VOUT1 voltage to the value of 3.3V typical. Connect this pin to HV Buck1 output voltage via short trace. |
| PGND1 | 15 | Power ground pin of HV Buck1. |
| SW1 | 16 | Regulator switching node of HV Buck1. Connect SW1 to an external power inductor. |

VIN

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$V_{IN}$=12V, $T_J$=-40°C~150°C, typical values are tested under 25°C.

| SYMBOL | PARAMETER | TEST CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **Power Supply and Output** | | | | | | |
| V | | | | | | |

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$V_{IN}$=12V, $T_J$=-40°C~150°C, typical values are tested under 25°C.

| SYMBOL | PARAMETER | TEST CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $R_{DSON_H1}$ | High-side MOSFET on-resistance | $V_{BOOT}$-$V_{SW}$=5V | | 75 | 150 | mÝ |
| $R_{DSON_L1}$ | Low-side MOSFET on-resistance | | | 50 | 120 | mÝ |
| $I_{LIM_HS1}$ | High-side power MOSFET current limit | | 4.2 | 5.2 | 6.2 | A |
| $I_{LIM_LSP1}$ | Low-side power MOSFET positive current limit | | 3.2 | 4.2 | 5.2 | A |
| $I_{LIM_LSN1}$ | Low-side power MOSFET negative current limit | | 0.8 | 2 | 3.2 | A |
| $R_{DIS1}$ | Discharge resistance | Output disabled | | 100 | 200 | Ý |
| $t_{ON_MIN1}$ | Minimum on-time | | | 80 | | ns |
| $d_{Phase1}$(1) | Switching phase | | | 0 | | deg |
| **VOUT2 (LV Buck)** | | | | | | |
| $V_{S2}$(1) | Supply voltage range | | 3 | | 5.5 | V |
| $V_{ACC2}$ | Voltage accuracy | $T_J$ = 25°C | -1 | | 1 | % |
| | | $T_J$ = -40°C~150°C | -1.5 | | 1.5 | % |
| $R_{DSON_H2}$ | High-side MOSFET on-resistance | | | 65 | 150 | mÝ |
| $R_{DSON_L2}$ | | | | | | |

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$V_{IN}$=12V, $T_J$=-40°C~150°C, typical values are tested under 25°C.

| SYMBOL | PARAMETER | TEST CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $R_{DIS3}$ | Discharge resistance | Output disabled | | 55 | 100 | Ý |
| $t_{ON_MIN3}$ | Minimum on-time | | | 90 | | ns |
| $d_{Phase3}$(1) | Switching phase | | | 180 | | deg |
| **VOUT4 (LDO)** | | | | | | |
| $V_{ACC4}$ | Voltage accuracy | VOUT4 set to 2.8V | -1.5 | | 1.5 | % |
| $V_{DROP_LDO}$ | LDO dropout voltage | VOUT1=3.3V, VOUT4=3.3V $I_{OUT4}$=400mA | | 120 | 300 | mV |
| $L_{DO_LINE_REG}$ | LDO line regulation | VOUT1=3.3V to 5V, VOUT4 set to 2.8V, $I_{OUT4}$=100mA | | 0.25 | | %/V |
| $L_{DO_LOAD_REG}$ | LDO load regulation | VOUT1=3.3V, VOUT4 set to 2.8V, $I_{OUT4}$=10mA to 400mA | | 0.05 | | % |
| $I_{LIM_LDO_OCP}$ | LDO over current limit | VOUT1=3.3V, VOUT4 set to 2.8V | 480 | 600 | 720 | mA |
| $I_{LIM_LDO_SCP}$ | LDO output short current limit | VOUT1=3.3V, VOUT4=0V | | 140 | | mA |
| $R_{DIS4}$ | Discharge resistance | Output disabled | | 100 | 200 | Ý |

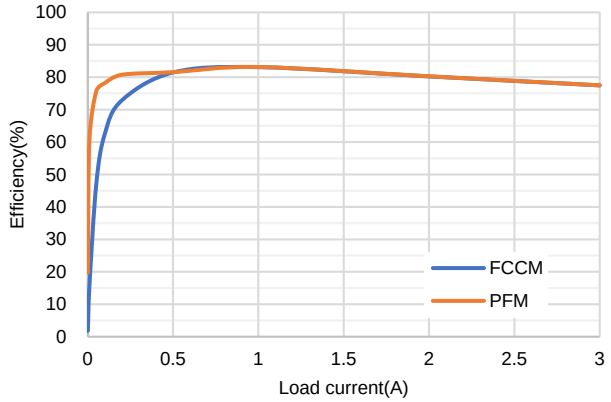
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$V_{IN}$=12V, $T_J$=-40°C~150°C, typical values are tested under 25°C.

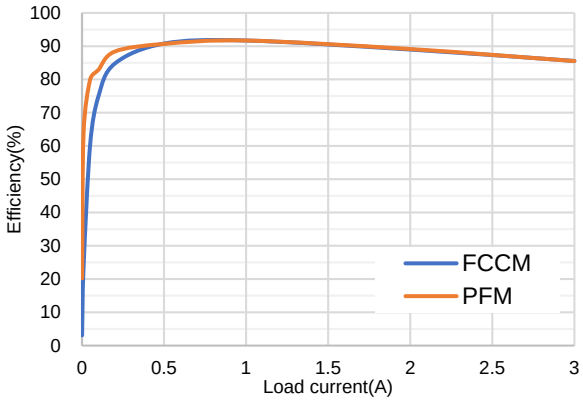
| SYMBOL | PARAMETER | TEST CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|

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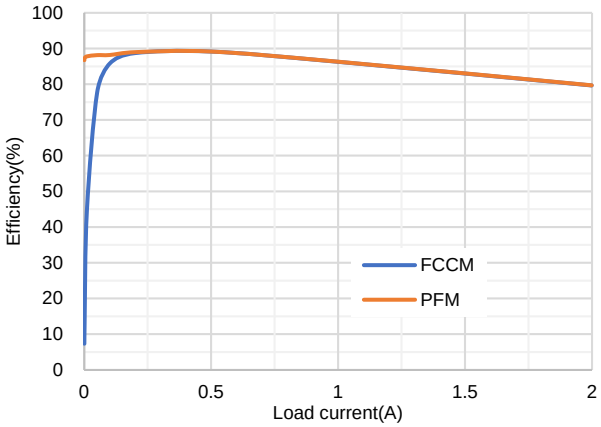
$V_{IN}$=12V, $T_J$=-40°C~125°C, unless otherwise noted.



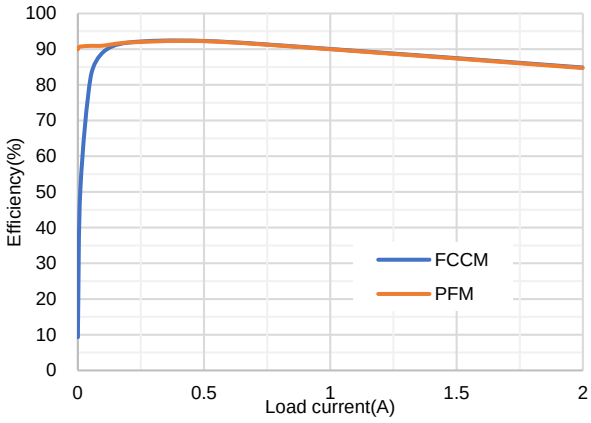

Buck1 Efficiency vs Load Current, $V_{OUT1}$=3.3V, $f_{SW1}$=2.2MHz



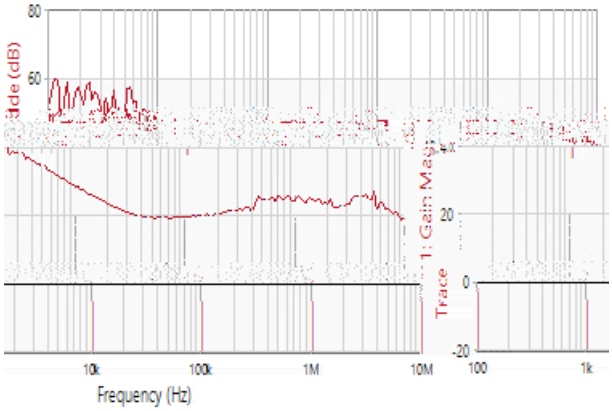

Buck1 Efficiency vs Load Current, $V_{OUT1}$=3.3V, $f_{SW1}$=400kHz




Buck2/3 Efficiency vs Load Current, $V_{OUT2/3}$=1.2V




Buck2/3 Efficiency vs Load Current, $V_{OUT2/3}$=1.8V

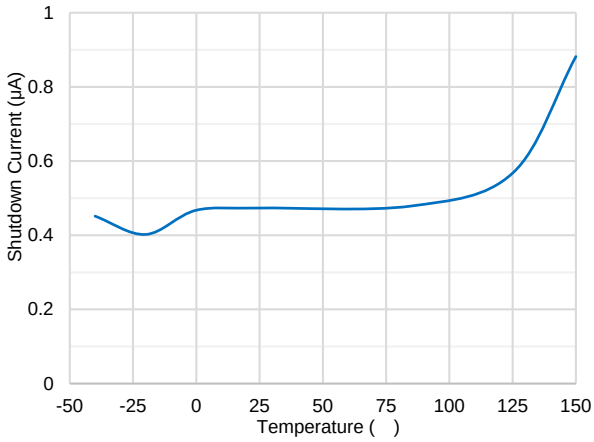



LDO PSRR, $V_{OUT4}$=2.8V, $I_{OUT4}$=10mA

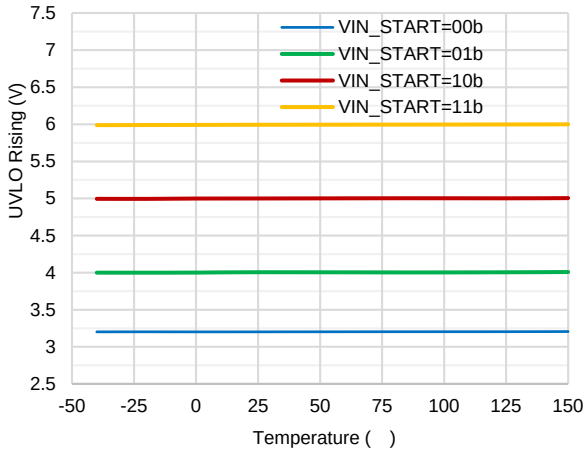
LDO PSRR, $V_{OUT4}$=2.8V, $I_{OUT4}$=100mA

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$V_{IN}$=12V, $T_J$=-40°C~125°C, unless otherwise noted.




Shutdown Current vs. Temperature




UVLO Rising Threshold vs. Temperature



UVLO Falling Threshold vs. Temperature

VCC vs. Temperature

Buck1 $R_{DSON_HS1}$ vs. Temperature

Buck1 $R_{DSON_LS1}$ vs. Temperature

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**Overview**

The SCT61441S device is a wide input power management IC with quad channels output. The device is designed for camera modules in automotive ADAS vision and DMS/OMS applications. The SCT61441S integrates one 3A HV Buck, two identical 2A LV Buck and a 400mA LV Low-Drop Regulator(LDO). Each channel output is continuously monitored, any over-voltage/under-voltage fault will trigger RESETB pull low. Any deep over-voltage/under-voltage will be detected and the device will enterunde

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### High Efficiency Regulators

The switching frequency of HV Buck is 2.2MHz/400kHz selectable. All the LV bucks employ 2.2MHz fixed frequency peak current mode control. Forced continuous conduction mode (FCCM) allows the device to have a high output performance when light load. Built-in UVLO ensures all channels are capable of regulated output under the operating VIN range. Soft-start is fixed at 1ms for all channels. VOUT1 will always be the firstly built rail after power on, the other rails can be configured with range 0ms to 75ms turn on delay. Then the device can achieve a variety of sequence to fit power system.

The VOUT1 is a HV synchronous buck converter directly power from VIN pin. It's regulated at 3.3V with up to 3A continuous current. An external 100nF ceramic bootstrap capacitor between BST and SW1 pin powers high-side power MOSFET gate driver. The bootstrap capacitor voltage is charged from an integrated voltage regulator when high-side power MOSFET is off and low-side power MOSFET is on. Note VOUT1 is the power supply for VOUT2/3/4.

The VOUT2 and VOUT3 are two identical LV synchronous buck converter power by VOUT1. Their output can be configured via I2C range from 0.8V to 2.35V with 50mV step. Each is capable of 2A continuous current. To further improve the EMI performance, the VOUT2 and VOUT3 will operate with 180° phase-shifted clock.

The VOUT4 is a low-drop regulator(LDO) also powered by VOUT1. The LDO output is factory-programmed at 1.8V, 2.7V, 2.8V, 2.9V or 3.3V with up to 400mA continuous output current.

The converters have proprietary designed gate driver scheme to resist switching node ringing without sacrificing MOSFET turn-on and turn-off time, which further erases high frequency radiation EMI noise caused by the MOSFETs hard switching.

Each output voltage is continuously monitored during operation, the OV/UV threshold can be adjusted independently in register **CONFIG_PGSEL1** and **CONFIG_PGSEL2**.

### Deep Over Voltage Protection

If any output exceeds the deep over voltage protection threshold 115%, all outputs will shut off for the hiccup time. When hiccup ends, the normal power up sequence will start again following turn on delay setting in register. When entry hiccup, the output discharge will operate during the hiccup time. The threshold can be configured by bits **DEEP_OVP_SEL[1:0]**.

### Deep Under Voltage Protection

If an output falls below the deep under voltage protection threshold 75%, all outputs will shut off for the hiccup time. When hiccup ends, the normal power up sequence will start again following turn on delay setting in register. When entry hiccup, the output discharge will operate during the hiccup time. The threshold can be configured by bits **DEEP_UVP_SEL[1:0]**.

### Thermal Shutdown

The

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pseudo modulation. Therefore, the SCT61441S can guarantee that the switching frequency does not drop into the 1.8MHz AM band limit.

**Frequency Foldback**

To avoid meeting minimum on time, the HV buck VOUT1 will reduce switching frequency actively when input voltage rising high. Other channel's frequency is unchanged. When VIN greatly drops and minimum off time of HV buck VOUT1 is kicked, the VOUT1 enter dropout mode and also reduce its frequency to get max output.

**RESETB Indicator**

The RESETB indicator will assert under reset e7.4 (s>4.7 6-1.6.9 (y)17.1T Td (-2 (er)-1.3 (10.6 (e)-2 (er)- (e)6.1 (udo )]TJ -0

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**Packet Error Checking (PEC)**

The SCT61441S supports optional packet error checking (PEC) byte during the I2C communication. PEC can significantly increase fault coverage on the I2C interface. The PEC byte is implemented through CRC-8 polynomial of x8 + x2 + x +1. The PEC byte does not take ACK, NACK, START, STOP, Repeated START bits into calculation. The PEC byte is calculated on the register address and data byte over the entire message from the first START condition, note that the slave address is removed both in write and read command. When PEC is enabled, the device will reject the write command if the master send an incorrect PEC byte. When in read mode with PEC enabled, the master should acknowledge the data byte thus then the device will send the PEC byte. The PEC can be configured by **PEC_EN** in register **CONFIG_FSS**.

**Write Data Format**

A write to the device includes transmission of the following:

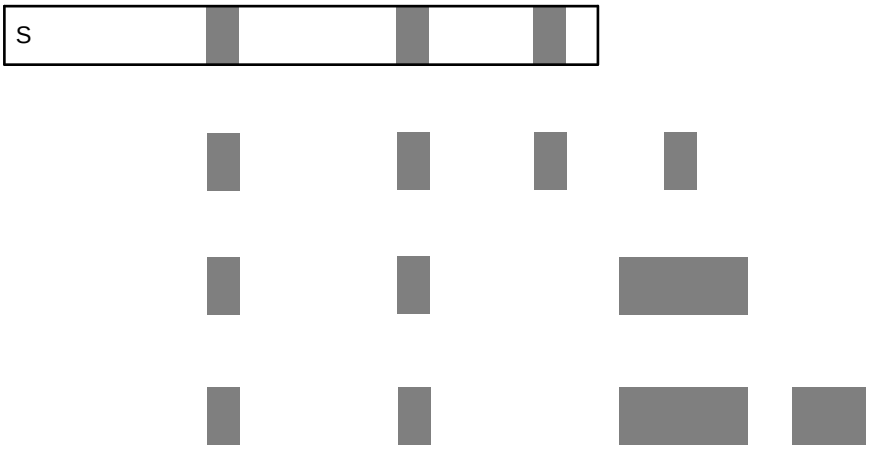
- START condition
- Slave address with the write bit set to 0
- 1 byte of data to register address
- 1 byte of data to the command register
- STOP condition

**Read Data Format**

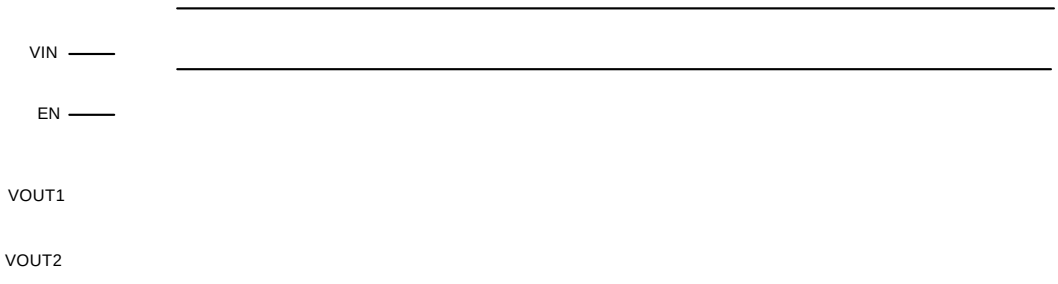
A read from the device includes the following:

- Transmission of a START condition
- Slave address with the write bit set to 0
- 1 byte of data to register address
- Restart condition
- Slave address with read bit set to 1
- 1 byte of data to the command register
- STOP condition

Figure 6 illustrates the proper format for one frame.




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# SCT61441S

**Under Voltage Lock-Out**

An external voltage divider network of $R_1$ from the input to EN pin and $R_2$ from EN pin to the ground can set a higher input voltage's Under Voltage Lock-Out (UVLO) threshold. The UVLO has two thresholdsW.4 ( )0(t)5 (n  Q  BT  /H3 3tf (o )0

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The total current flowing through the inductor is the inductor ripple current plus the output current. When selecting an inductor, choose its rated current especially the saturation current larger than its peak operation current and RMS current also not be exceeded. Therefore, the peak switching current of inductor, $I_{LPEAK}$ and $I_{LRMS}$ can be calculated as in equation 5 and equation 6.

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**Bootstrap Capacitor Selection**

A 0.1εF ceramic capacitor must be connected between BST pin and SW1 pin for proper operation. A ceramic capacitor with X5R or better grade dielectric is recommended. The capacitor should have a 10V or higher voltage rating.

**Output Capacitor Selection**

The selection of output capacitor will affect output voltage ripple in steady state and load transient performance.

For buck converter, the output ripple is essentially composed of two parts. One is caused by the inductor current ripple going through the Equivalent Series Resistance ESR of the output capacitors and the other is caused by the inductor current ripple charging and discharging the output capacitors. To achieve small output voltage ripple, choose a low-ESR output capacitor like ceramic capacitor. For ceramic capacitors, the capacitance dominates the output ripple. For simplification, the output voltage ripple can be estimated by Equation 10 desired.

$$\Delta V_{OUT_BUCK} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{8 \times f_{SW} \times L \times C_{OUT} \times V_{IN}} \quad (10)$$

Where

- $\Delta V_{OUT_BUCK}$ is the output voltage ripple of buck converter
- $f_{SW}$ is the switching frequency
- L is the inductance of inductor
- $C_{OUT}$ is the output capacitance
- $V_{OUT}$ is the output voltage
- $V_{IN}$ is the input voltage

Due to capacitor's degrading under DC bias, the bias voltage can significantly reduce capacitance. Ceramic capacitors can lose most of their capacitance at rated voltage. Therefore, leave margin on the voltage rating to ensure adequate effective capacitance. Typically, two 10εF ceramic output capacitors work for most applications.

**Table 3. Recommended BOM for Typical Application**

| Output Rail | Frequency (MHz) | L (uH) | Input Capacitor (uF) | Output Capacitor (uF) |
|---|---|---|---|---|
| Buck1 | 2.2 | 2.2 | 2 x 10+1 x 0.1 | 2 x 22 |
| Buck2 | 2.2 | 1 | [redacted] | 2 x 22 |
| Buck3 | 2.2 | 1 | 10+1 x 0.1 | 22 x |

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**Layout Guideline**

Proper PCB layout is a critical for device's stable and efficient operation. The traces conducting fast switching currents or voltages are easy to interact with stray inductance and parasitic capacitance to generate noise and degrade performance. For better results, follow these guidelines as below:

1. Power grounding scheme is very critical because of carrying power, thermal, and glitch/bouncing noise associated with clock frequency. The rule of thumb is to make ground trace lowest impendence and power are distributed evenly on PCB. Sufficiently placing ground area will optimize thermal and not causing over heat area.

2. Make sure the ground path between VIN capacitor and PGND1 pin is shortest with lowest impendence.

3. Place a low ESR ceramic capacitor as close to VIN1 and VIN23 pin and the ground as possible to reduce parasitic effect.

4. For operation at full rated load, the top side ground area must provide adequate heat dissipating area. Make sure top switching loop with power have lower impendence of grounding.

5. The bottom layer is a large ground plane connected to the ground plane on top layer by vias. The power pad should be connected to bottom PCB ground planes using multiple vias.

6. Output inductor should be placed close to the SW pin. The switching area of the PCB conductor minimized to prevent excessive capacitive coupling.

7. EN UVLO adjust resistors and feedback trace should connect to small signal ground which must return to the GND pin without any interleaving with power ground.

8. For achieving better thermal performance, a four-layer layout is strongly recommended.

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C

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| | | | | |
|---|---|---|---|---|
| | | | | 10: Scale=2.5ms. Delay ranges from 0-37.5ms<br>11: Scale =5ms. Delay ranges from 0-75ms |

| **CONFIG_T2 [7:0]** | | | | |
|---|---|---|---|---|
| **ADDRESS:** 0x03 | | | | |
| **BITS** | **FIELD** | **TYPE** | **DESCRIPTION** | **DECODE** |
| [7:6] | RESERVED | R | / | / |

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| | | | | |
|---|---|---|---|---|
| [7:4] | ON_DELAY3 | W/R | OUT3 Power-Up and Recover Turn On delay. | when DELAY_SCALE=00, $t_{ON_DELAY3}$ = ON_DELAY3[3:0] x 0.5ms<br>when DELAY_SCALE=01, $t_{ON_DELAY3}$ = ON_DELAY3[3:0] x 1ms<br>when DELAY_SCALE=10, $t_{ON_DELAY3}$ = ON_DELAY3[3:0] x 2.5ms<br>when DELAY_SCALE=11, $t_{ON_DELAY3}$ = ON_DELAY3[3:0] x 5ms |
| [3:0] | ON_DELAY2 | W/R | OUT2 Power-Up and Recover Turn On delay. | when DELAY_SCALE=00, $t_{ON_DELAY2}$ = ON_DELAY2[3:0] x 0.5ms<br>when DELAY_SCALE=01, $t_{ON_DELAY2}$ = ON_DELAY2[3:0] x 1ms<br>when DELAY_SCALE=10, $t_{ON_DELAY2}$ = ON_DELAY2[3:0] x 2.5ms<br>when DELAY_SCALE=11, $t_{ON_DELAY2}$ = ON_DELAY2[3:0] x 5ms |

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| | | | |
|---|---|---|---|
| [5] | UV_WAR4 | Read Clear | UV warning for OUT4, |

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[5] OFF4

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| | | | | |
|---|---|---|---|---|
| | | | | If configured as a QA watchdog, writing the incorrect response to the WDKEY register will result in the value written being ignored and a WD_LFSR violation. Writing the correct response in QA mode during an open window will result in a refresh and the WDKEY register being updated. Writing the correct response in QA mode during a closed window will result in the write being ignored and a WD_UV violation.<br>LFSR polynomial: x8 + x6 + x5 + x4 + 1 |

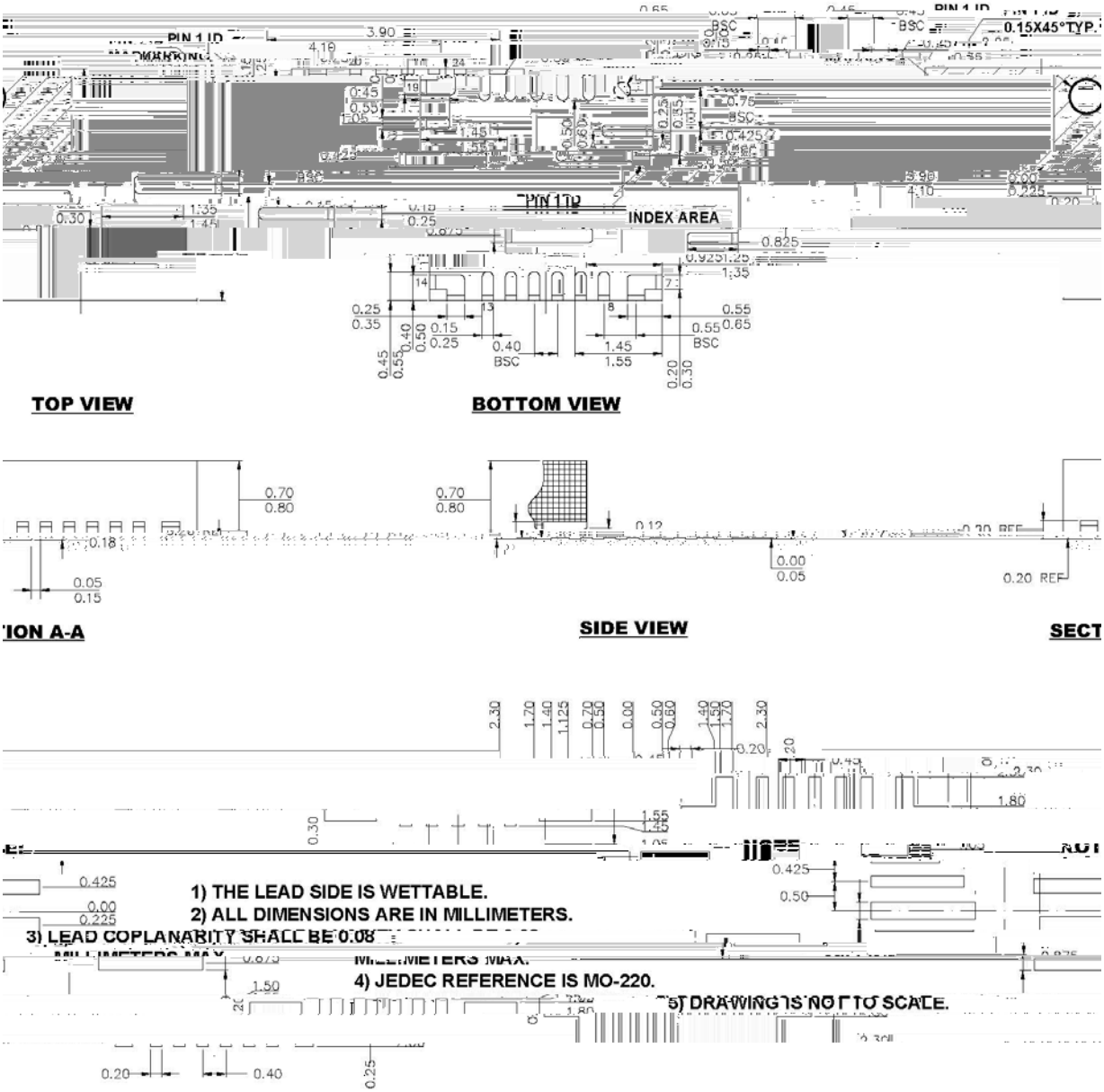
| **WD_LOCK [7:0]** | | | | |
|---|---|---|---|---|
| **ADDRESS:** 0x17 | | | | |
| **BITS** | **FIELD** | **TYPE** | **DESCRIPTION** | **DECODE** |
| [7:1] | RESERVED | R | / | / |
| [0] | WDLOCK | W/R | Watchdog Lock Protection | 0 = Watchdog configuration registers are writeable<br>1 = Watchdog configuration registers are read-only |

**CONFIG_PGSEL1**

| | | | | |
|---|---|---|---|---|
| [0] | I2C_LOCK | W/R | Lock Protection. If 0 by default, then this bit can be changed through the I2C. | 0 = All registers can be written.<br>1 = Writes are ignored to protected registers. |

| **SYS_STATE [7:0]** |
|---|
| **ADDRESS:** 0x22<br>**BITS F** |

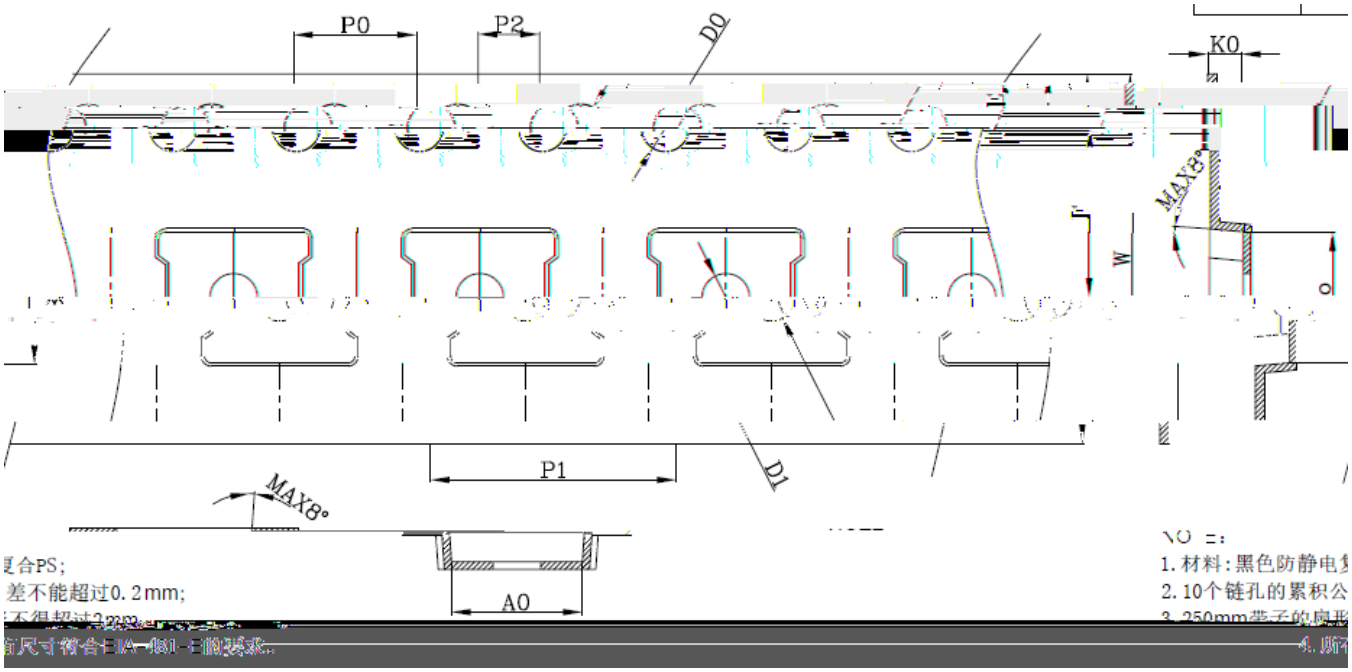
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| SYMBOL | A0 | B0 | K0 | P0 | P1 | P2 |
|---|---|---|---|---|---|---|
| 10±0.10 | 4.00±0.10 | 8.00±0.10 | 2.00±0.05 | SPEC | 4.30±0.10 | 4.30±0.10 |
| SYMBOL | D0 | D1 | T | SYMBOL | E | W |
| 30±0.05 | 1.55±0.05 | 1.55±0.10 | 10.00±0.30 | SPEC | 0.30±0.05 | 16.00±0.30 |

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