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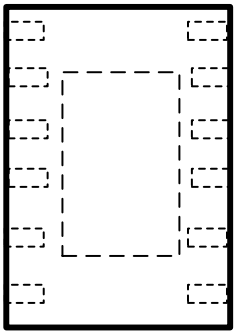
NOTE: Page numbers for previous revisions may differ from page numbers in the current version

Revision 1.0: Released to market.
Revision 1.1: Updated “TAPE AND REEL INFORMATION” on page 33.
Revision 1.2: Updated Package Description from “TQFN2X3-12L” to “DFN2X3-12L”.

SCT81623QDPAR	Tape & Reel	5000	1623Q	12	DFN2X3-12L	1

Over operating free-air temperature unless otherwise noted(1)

BIAS, UVLO/EN/SYNC	-0.3	62	



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V_{BIAS}=12V, T_J=-40℃~150℃, typical values are tested under 25℃.

V_{BIAS}	Operating input voltage		3.1	60	V
V_{BIAS_UVLO}	BIAS Input UVLO	V_{BIAS} rising	2.82	3	V
	Hysteresis		160		

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V_{BIAS}=12V, T_J=-40℃~150℃, typical values are tested under 25℃.

V_{CS_THR}	Current sense threshold		82	100	118	mV
V_{SL}(2)	Internal compensation Ramp voltage			90		mV
$C_{HICC-DEL}$	Hiccup mode activation delay	Clock cycles with current limiting before hiccup off-time activated (SS_done)		64		cycles
C_{HICCUP}	Hiccup mode off-time after activation	Clock cycles with no switching followed by SS release		32768		cycles
I_{SS}	Soft-start current		7	10	14	μA
R_{SS}	SS pull-down switch R_{DSON}			65		Ω
R_{PG}	PG pulldown switch resistance	1mA sinking		120		Ω
V_{UVTH}	PG under-voltage threshold	FB rising (Reference to V_{REF})	92	95	98	%
		FB falling (Reference to V_{REF})	87	90	93	%
		FB Hysteresis		5		%
F_{SW}	Switching frequency	R_{RT}=47.5kΩ	400	456	510	kHz
F_{SS}	Frequency Spread Range					

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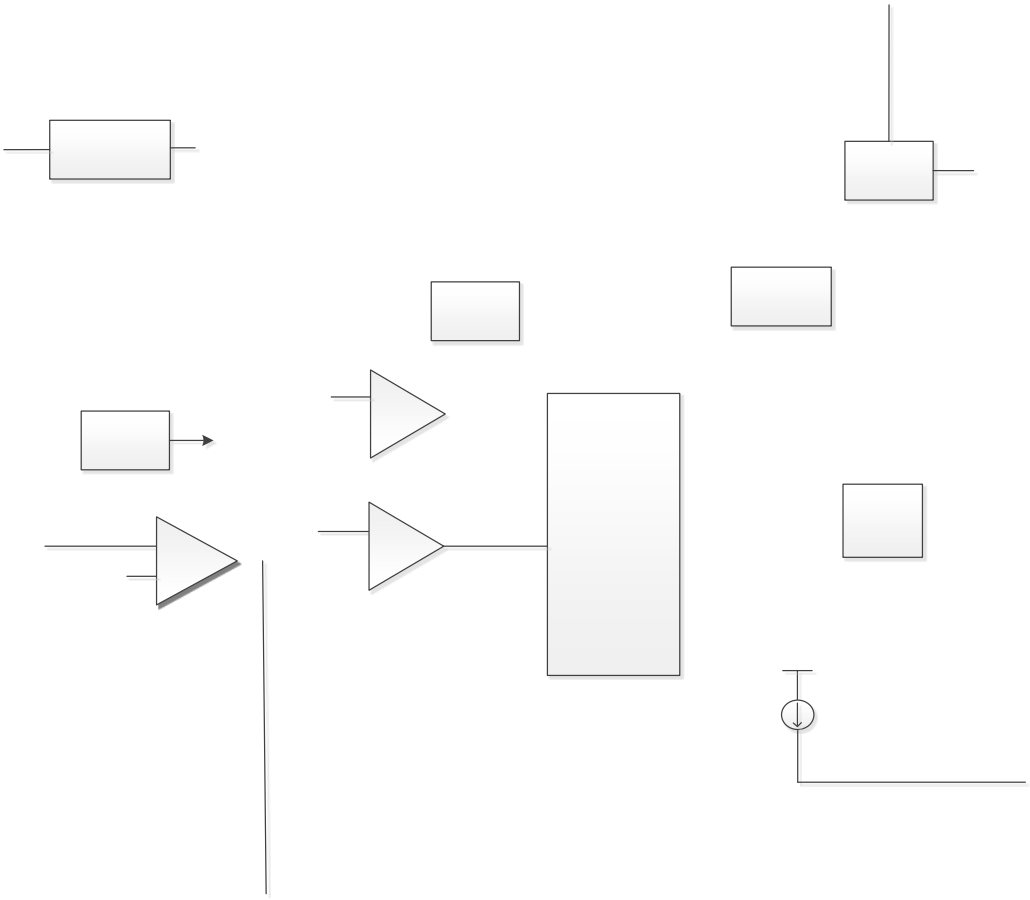


Figure 12. Functional Block Diagram

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The SCT81623Q device is a wide input range, non-synchronous boost controller that uses peak-current-mode control. The device can be used in boost, SEPIC and flyback topologies.

In a typical application circuit, the peak current through the external MOSFET is sensed through an external sense resistor. The voltage across this resistor is fed into the CS pin. This voltage is fed into the positive input of the PWM comparator. The output voltage is also sensed through an external feedback resistor divider network and fed into the error amplifier negative input. The output of the error amplifier (COMP pin) is added to the slope compensation ramp and fed into the negative input of the PWM comparator. At the start of any switching cycle, the oscillator sets the RS latch using the switch logic block. This forces a high signal on the GATE pin (driver of the external MOSFET) and the external MOSFET turns on. When the voltage on the positive input of the PWM comparator exceeds the negative input, the RS latch is reset and the external MOSFET turns off. The voltage sensed across the sense resistor generally contains spurious noise spikes. These spikes can force the PWM comparator to reset the RS latch prematurely. To prevent these spikes from resetting the latch, a blank-out circuit inside the IC prevents the PWM comparator from resetting the latch for a short duration after the latch is set. This duration is called the blanking interval and is specified as minimum on-time in the Electrical Characteristics section. Under extremely light-load or no-load conditions, the energy delivered to the output capacitor when the external MOSFET in on during the blanking interval is more than what is delivered to the load. An over-voltage comparator inside the SCT81623Q prevents the output voltage from rising under these conditions. The over-voltage comparator senses the feedback (FB pin) voltage and resets the RS latch. The latch remains in reset state until the output decays to the nominal value.

The SCT81623Q works at pulse skip mode (PSM) to further increase the efficiency in light load condition.

The quiescent current of SCT81623Q is 540μA typical under no-load condition and no switching. Disabling the device, the typical supply shutdown current on BIAS pin is 3.6μA.

The SCT81623Q has over voltage protection (OVP) for the output voltage. OVP is sensed at the feedback pin (FB). If at any time the voltage at the feedback pin rises to 1.1V (typ.), OVP is triggered. OVP will cause the GATE pin to go low, forcing the power MOSFET off. With the MOSFET off, the output voltage will drop. The SCT81623Q begins switching again when the feedback voltage reaches 1.05V (typ.).

The SCT81623Q uses a current mode control scheme. The main advantages of current mode control are inherent cycle-by-cycle current limit for the switch and simpler control loop characteristics. However, current mode control has a Sub-harmonic Oscillation when duty cycle is greater than 50%. To prevent the Sub-harmonic oscillations, a compensation ramp is added to the control signal.

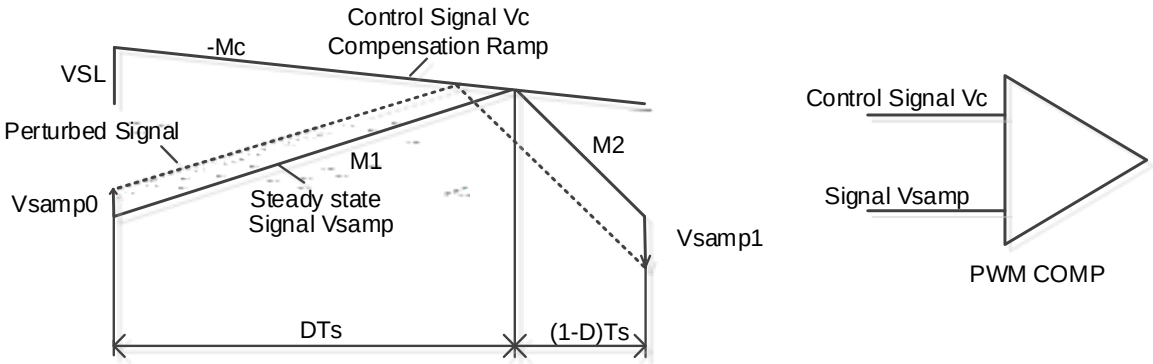


Figure 13. Sub-Harmonic Oscillation for D>0.5 and Compensation Ramp to Avoid Sub-Harmonic Oscillation

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The current mode control scheme samples the inductor current, IL, and compares the sampled signal, V_{samp}, to a internally generated control signal, V_C. The current sense resistor, R_{SEN}, as shown in Figure13

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A typical value for factor K is 40 μA.

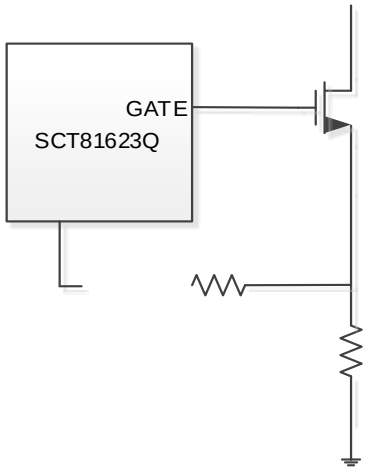


Figure14. External R_{SL} to increase slope compensation

The device provides cycle-by-cycle peak current limit protection that turns off the MOSFET when the sum of the inductor current and the programmable slope compensation ramp reaches the current limit threshold. Peak inductor current limit ($I_{PEAK-CL}$) in steady state is calculated as shown in:

$$I_{PEAK_CL} \quad \frac{V_{SENSE} \quad uA \quad R_{SL} \quad D}{R_{SEN}} \tag{11}$$

Where

V_{CS_THR} is CS pin limiting voltage (Typ. =100mV)
$I_{PEAK-CL}$ is the inductor peak current limit
R_{SL} is Slope compensation resistor
D is Duty cycle
R_{SEN} is the Inductance peak current detection resistance

If required, a small external RC filter (R_F, C_F) at the CS pin can be added to overcome the large leading-edge spike of the current sense signal. Select an R_F value in the range of 10 Ω to 200 Ω and a C_F value in the range of 100 pF to 2nF. Because of the effect of this RC filter, the peak current limit is not valid when the on-time is less than 2 × R_F × C_F. To fully discharge the C_F during the off-time, the RC time constant should satisfy the following inequality.

$$R_F \quad C_F \quad \frac{D}{F_S} \tag{12}$$

When overload happens, the converter cannot provide output current to satisfy loading requirement. The inductor current is clamped at over current limitation. Thus, the output voltage drops below regulated voltage with FB voltage less than internal reference voltage continuously. The internal COMP voltage ramps up to high. When COMP voltage is clamped for 64 cycles, the controller stops working. After remaining OFF for 32768 cycles the device restarts from soft starting phase. If overload or hard short condition still exists during soft-start and make COMP voltage clamped at high after soft start time and COMP still keep high for 64 cycles the device enters into turning-off mode again. When overload or hard short condition is removed, the device automatically recovers to enter normal regulating operation.

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64 cycles of

Figure 15. Hiccup Mode Protection

Because D can be variable under different V_{BIAS}, $I_{PEAK-CL}$ is not stable under different V_{BIAS} when using external slope compensation resistor. So, for an accurate peak current limit operation over the input supply voltage, SCT recommends using only the fixed slope compensation.

The output voltage is set by an external resistor divider R_{FBT} and R_{FBB} in typical application schematic. The value of R_{FBT} can be calculated by equation 13.

$$R_{FBT} \quad \frac{V_{OUT} \quad V_{REF}}{V_{REF}} \quad R_{FBB} \tag{13}$$

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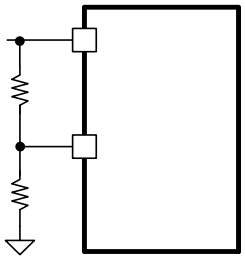


Figure 17. System UVLO Resistor Divider

When the UVLO pin voltage is above the UVLO threshold, the device enters run mode. In run mode, a soft-start sequence starts after 8 clocks once the VCC voltage exceeds the 2.85V VCC UV threshold. UVLO hysteresis is accomplished with an internal 50mV voltage hysteresis and an additional 5μA current source that is switched on or off. When the UVLO pin voltage exceeds the UVLO threshold, the current source is enabled to quickly raise the voltage at the UVLO pin. When the UVLO pin voltage falls below the UVLO threshold, the current source is disabled, causing the voltage at the UVLO pin to fall quickly. When the UVLO pin voltage is less than the enable threshold, the device enters shutdown mode after a 30μs (typ.) delay with all functions disabled.

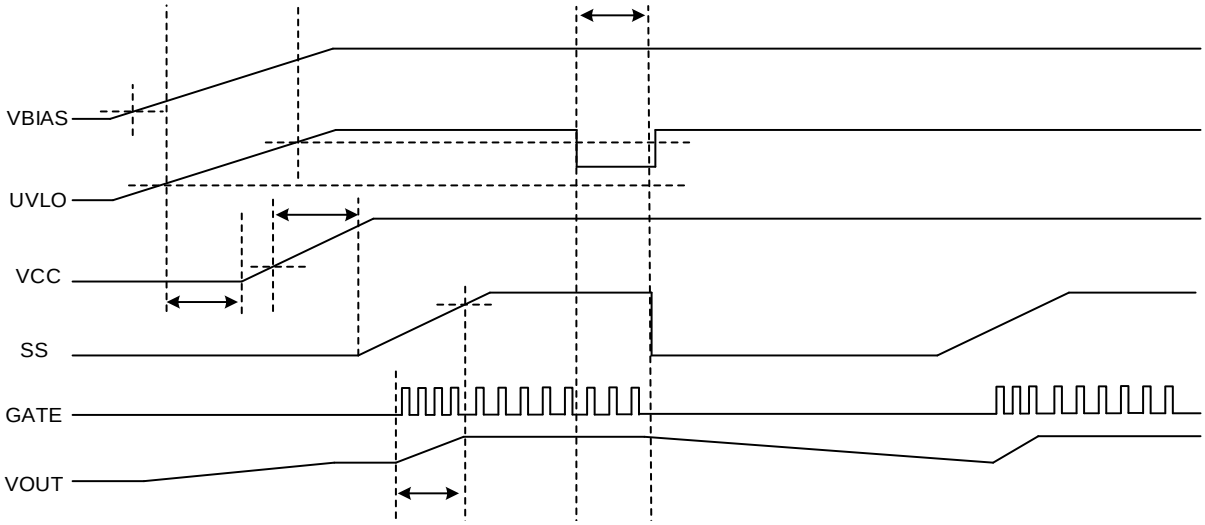


Figure 18. Boost Start-Up Waveforms Case 1: Start-Up diagram, UVLO Toggle After Start-Up

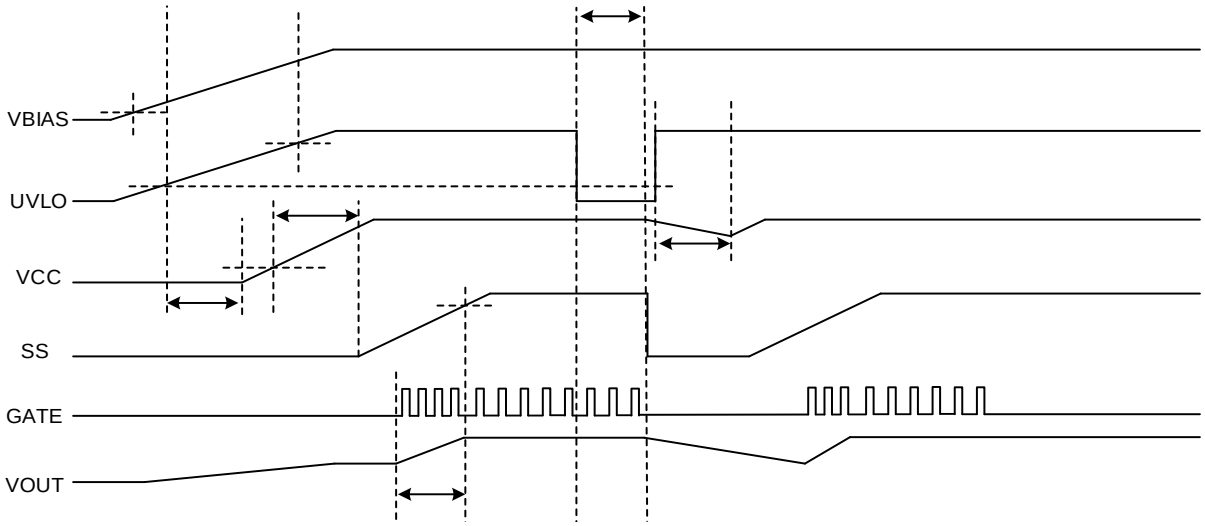


Figure 19. Boost Start-Up Waveforms Case 2: Start-Up diagram, EN Toggle After Start-Up

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The switching frequency of the device can be synchronized to an external clock by pulling doQ EMC /Artifact <</Attached /Bot

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The performance of inductor affects the power supply's steady state operation, transient behavior, loop stability,

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The input capacitor should be capable of handling the RMS current. Although the input capacitor is not as critical in a boost application, low values can cause impedance interactions. Therefore, a good quality capacitor should be chosen in the range of 10μF to 40μF. If a value lower than 10μF is used, then problems with impedance interactions or switching noise can affect the SCT81623Q. To improve performance, especially with VBIAS below 8V, it is recommended to use a 2.2

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Where

G

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V_{BIAS}=12V, V_{OUT}=24V, unless otherwise noted

Figure 22. Power up (I_{LOAD}=2A)

Figure 23. Power down (I_{LOAD}

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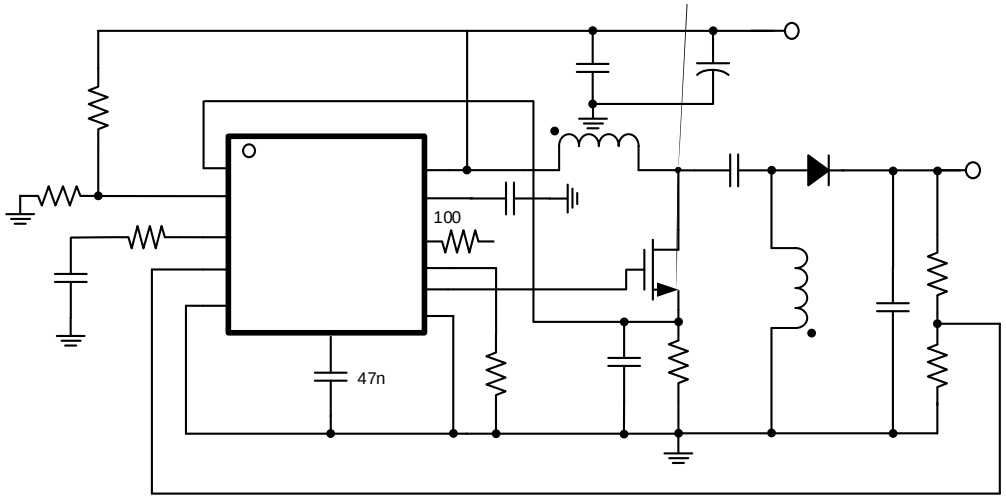


Figure 28. Application Schematic, 5V to 48V Input, 2A Sepic Regulator at 456kHz

Input Voltage	24V Normal 5 to 48V
Output Voltage	12V
Maximum Output Current	2A
Switching Frequency	456kHz
Output voltage ripple (peak to peak)	75mV (Load=2A)

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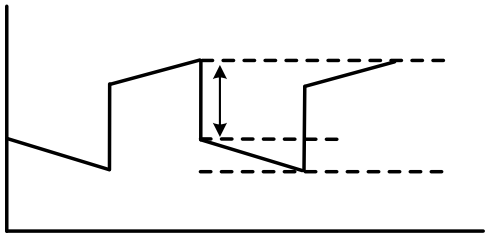


Figure 29. Output Voltage Ripple

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The peak primary winding current occurs at the minimum supply voltage as below equation:

$$I_{L_PEAK} \quad I_{LM} \quad \frac{I_{LM}}{} \quad \frac{P_O}{V_{INMIN} \quad D_{MAX}} \quad \frac{V_{INMIN} \quad D_{MAX}}{L_P \quad f_S} \tag{52}$$

The calculated turns ratio, primary winding inductance and peak current can be used to determine the magnetic core of the transformer, number of turns on primary and secondary windings, as well as wire thickness.

The voltage rating of the MOSFET and the diode need to be chosen with appropriate margin as both of them suffer from high voltage spikes. In case of MOSFET, the primary leakage inductance resonates with output capacitance of MOSFET and similarly in case of diode, secondary leakage inductance resonates with diode capacitance and results into high voltage spikes. Considering the spike voltage, usually choose 1.5~2 times of the voltage stage as the voltage rating to ensure sufficient margin.

The voltage rating of MOSFET and diode could be derived as shown in the equation below:

$$V_{ds_MOS} \qquad V_{IN_MAX} \quad \frac{N_P}{N_S} \quad V_O \tag{53}$$

$$V_{R_diode} \qquad V_{IN_MAX} \quad \frac{N_S}{N_P} \quad V_O$$

The current RMS rating of MOSFET could be derived as shown in below equation:

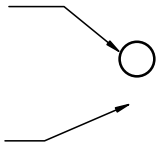
$$\sqrt{\quad \frac{}{} \quad \frac{}{} \quad}$$

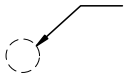
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The input capacitors smooth the supply ripple voltage during operation. Below equation is used to estimate the required input capacitor based on the supply ripple voltage specification.

$$C_{IN} \quad \frac{\frac{P_O}{V_{IN_MIN}} \quad D}{f_{SW} \quad V_{SUPPLY}} \tag{57}$$

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