/ / 0- □

K B	MFK	MFK C K FL K
VOUT	1	Power output, please use as large an output capacitor as possible to reduce output voltage ripple
FB	2	Buck converter output feedback sensing voltage. Connect a resistor divider from VOUT to FB to set up output voltage. The device regulates FB to the internal reference of 0.8V typical.
EN	3	Enable logic input. The device has precision enable thresholds 1.215V rising / 1.12V falling for programmable UVLO threshold and hysteresis. The voltage applied to this pin must not exceed 6.5V.
BST	4	Power supply for the high-side power MOSFET gate driver. Must connect a 0.1µF or greater ceramic capacitor between BST pin and SW node.
SW	5	Power Switching Output. SW is the switching node that supplies power to the output. Note that a capacitor is required from SW to BST to power the high-side switch.
VIN	6	Power supply input. VIN supplies the power to the IC, as well as the step-down converter switches. Drive VIN with a 4.2V to 17V power source. Bypass VIN to GND with a suitably large capacitor to eliminate noise on the input to the IC. See Input Capacitor.
PGND	7	Power ground. Must be soldered directly to ground plane.

Over operating free-air temperature range unless otherwise noted

M B B	ABCFKF FL K	FK		KF
V_{IN}	Input voltage range	4.2	17	V
T_J	Operating junction temperature	-40	125	℃

M B B	ABCFKF FL K	FK		KF
V_{ESD}	Human Body Model(HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins(1)	-2	+2	kV
	Charged Device Model(CDM), per ANSI-JEDEC-JS-002-2014specification, all pins(1)	-0.5	+0.5	kV

(1) HBM and CDM stressing are done in accordance with the ANSI/ESDA/JEDEC JS-001-2014 specification

M B B	EB I B F	4I B I D / 2 . 4 &	KF
$R_{\theta JA}$	Junction to ambient thermal resistance(1)	83.16	℃/W
$R_{\theta JC\ (top)}$	Junction to case (top) thermal resistance(1)	86.10	
$R_{\theta JB}$	Junction to board thermal resistance(1)	14.06	
$R_{\Psi jt}$	Junction-to-top characterization parameter	18.24	

(1) SCT provides $R_{\theta JA}$ and $R_{\theta JC}$ numbers only as reference to estimate junction temperatures of the devices. $R_{\theta JA}$ and $R_{\theta JC}$ are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT2230M are mounted, and external environmental factors. The PCB board is a heat sink that is soldered

to the leads and thermal pad of the SCT2230M. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual $R_{\theta JA}$ and $R_{\theta JC}$.

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V_{IN}=12V, T_J=-40℃~125℃, typical values are tested under 25℃.

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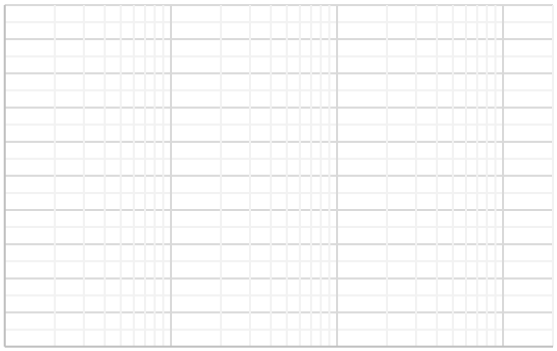


Figure 1. Efficiency vs Load Current(VIN=7.2V)

Figure 2. Efficiency vs Load Current(VIN=11.1V)

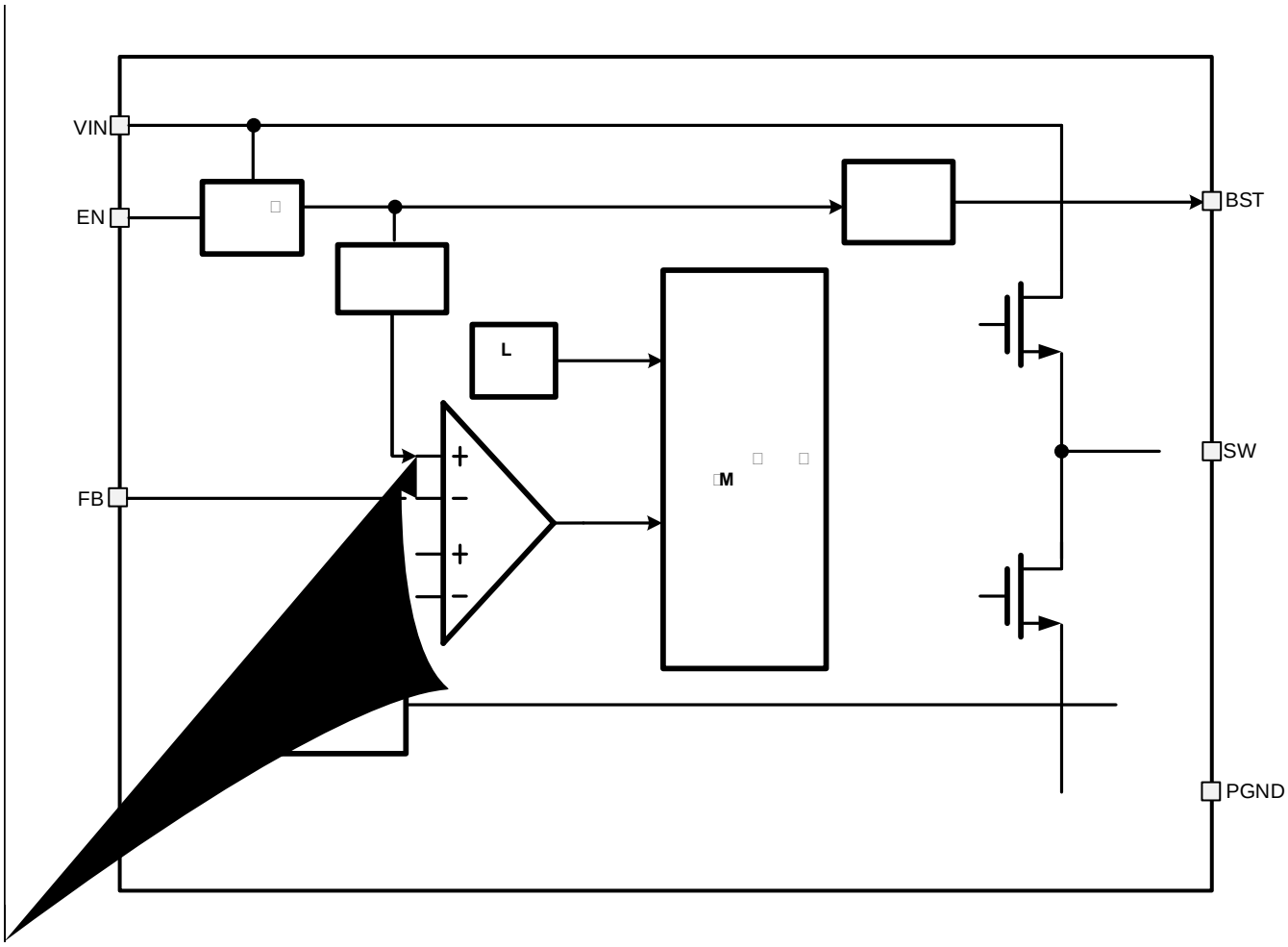
Figure 3. Load Regulation

Figure 4. FB Voltage Vs. Temperature

Figure 5. UVLO Vs. Temperature

Figure 6. Thermal Derating, VIN=12V (θ_{JA}=60℃/W)

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VIN
EN
FB
BST
SW
PGND
L
M

L

The SCT2230M device is 4.2-17V input, 2A output, synchronous step-down converter module with internal power MOSFETs. Adaptive constant on-time (ACOT) control is employed to provide fast transient response and easy loop stabilization. At the beginning of each cycle, the high-side MOSFET is turned on for a fixed one shot time ON

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triggered and the controller keeps the OFF state. A new switching cycle will begin only when the measured voltage is higher than limit voltage. If output loading continues to increase, output will drop below the UVP, and SS pin is discharged such that output is 0V. Then the device will count for 7 cycles of soft-start time for hiccup waiting time and restart normally after 7 cycles' soft-start period.

An external bootstrap capacitor between BST and SW pin powers floating high-side power MOSFET gate driver. The bootstrap capacitor voltage is charged from an integrated voltage regulator when high-side power MOSFET is off and low-side power MOSFET is on.

Once the junction temperature in the SCT2230M exceeds 155°C, the thermal sensing circuit stops converter switching and restarts with the junction temperature falling below 130°C. Thermal shutdown prevents the damage on device during excessive heat and power dissipation condition.

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F

For good input voltage filtering, choose low-ESR ceramic capacitors. A ceramic capacitor 10μF is recommended for the decoupling capacitor and a 0.1μF ceramic bypass capacitor is recommended to be placed as close as possible to the VIN pin of the SCT2230M.

Use Equation (5) to calculate the input voltage ripple:

(5)

Where:

C_{IN} is the input capacitor value
f_{sw} is the converter switching frequency
I_{OUT} is the maximum load current

Due to the inductor current ripple, the input voltage changes if there is parasitic inductance and resistance between the power supply and the VIN pin. It is recommended to have enough input capacitance to make the input voltage ripple

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Vin=12V, Vout=3.3V, unless otherwise noted

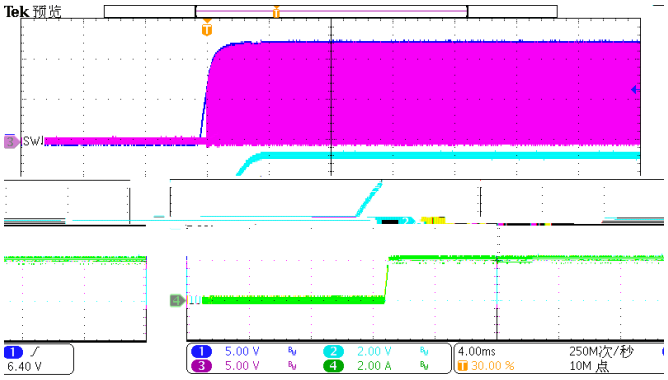


Figure 9. Power up(Iload=2A)

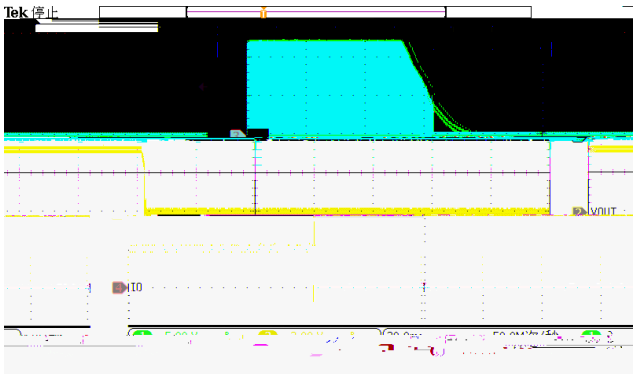


Figure 10. Power down(Iload=2A)

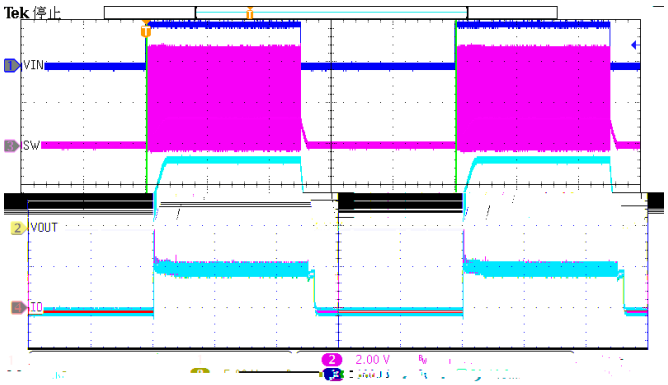


Figure 11. EN toggle (Iload=0.1A)

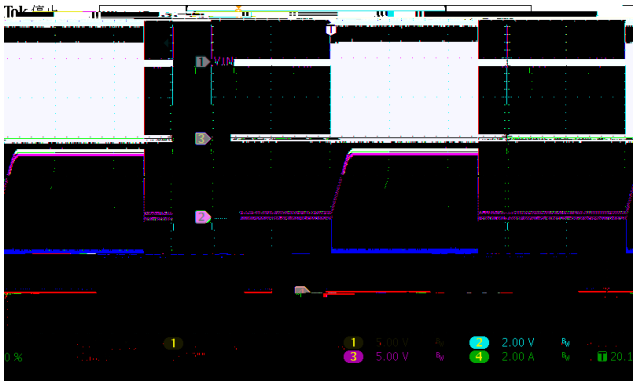


Figure 12. EN toggle (Iload=2A)

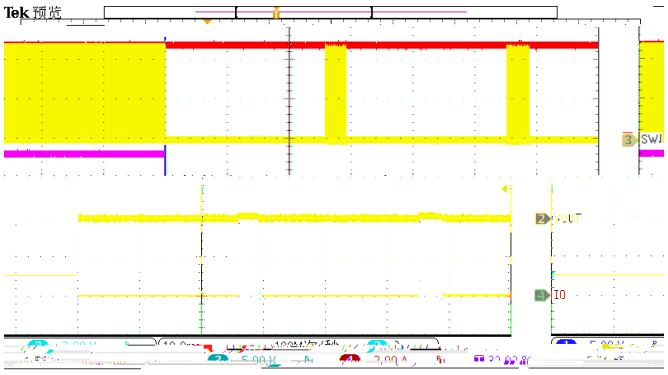


Figure 13. Over Current Protection(1A to hard short)

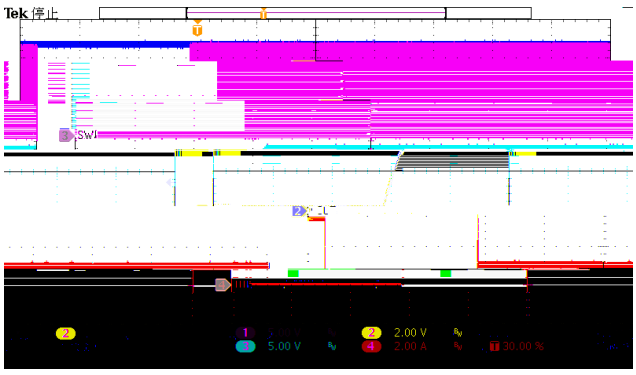


Figure 14. Over Current Release (hard short to 1A)

Figure 15

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The maximum IC junction temperature should be restricted to 125℃ under normal operating conditions. Calculate the maximum allowable dissipation, $P_{D(max)}$, and keep the actual power dissipation less than or equal to $P_{D(max)}$. The maximum-power-dissipation limit is determined using Equation (9).

(9)

where

T_A

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L I			
	176	178	330
K	58	60	62
.	124	-	-